HP 12966A
BUFFERED ASYNCHRONOUS DATA COMMUNICATIONS INTERFACE
Installation and Reference Manual

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PRINTING HISTORY

The Printing History below identifies the Edition of this Manual and any Updates that are included. Periodically, update packages are distributed which contain replacement pages to be merged into the manual, including an updated copy of this Printing History page. Also, the update may contain write-in instructions.

Each reprinting of this manual will incorporate all past updates; however, no new information will be added. Thus, the reprinted copy will be identical in content to prior printings of the same edition with its user-inserted update information. New editions of this manual will contain new information, as well as all updates.

To determine what manual edition and update is compatible with your current software revision code, refer to the appropriate Software Numbering Catalog, Software Product Catalog, or Diagnostic Configurator Manual.

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PREFACE

This manual describes the Hewlett-Packard 12966A Buffered Asynchronous Data Communications Interface and provides installation instructions and programming information.

We assume that you are using this manual to code driver subroutines for this interface kit. You should know the following:

- RTE Assembler Language programming, especially I/O programming, including interrupt and direct memory access (DMA) or dual channel port controller (DCPC) operations. Refer to your RTE Assembler Reference Manual, for information.
- Computer data communications concepts.
- Your application, system organization, line protocol, and data communications equipment operation.

You will find useful information in the following publications:

- HP Data Communications Training Manual part no. 22999-90010. (This training manual presents the basic concepts of synchronous and asynchronous data communications.)
- HP Data Communications Modems Training Manual, part no. 22999-90013. (This training manual presents the concepts of data communications modems.)
- Data Sets 103A3, 103E, 103G, and 103H Interface Specification; Bell System Data Communications Technical Reference, publication no. 41102, October 1973. (This publication gives you information on the data set interface requirements.)
- Data Set 113A Interface Specification; Bell System Data Communications Technical Reference, publication no. 41104, August 1973. (This publication gives you information on the data set interface requirements.)
- Data Sets 202C and 202D Interface Specification; Bell System Data Communications Technical Reference, publication no. 41202, May 1964. (This publication gives you information on the data set interface requirements.)
- EIA Standard RS-232-C: Interface Between Data Terminal Equipment and Data Communications Equipment Employing Serial Binary Data Interchange August 1969. (This publication describes the function of the control and status lines used in data communications and line protocol.)
- Martin, James. Telecommunications and the Computer. Englewood Cliffs: Prentice-Hall, Inc., 1969. (This text gives a description of the world's telecommunications links and their uses for data transmission.)

- Martin, James. **Teleprocessing Network Organization.**. Englewood Cliffs: Prentice-Hall, Inc., 1970. (This text explains the many types of devices and procedures for controlling and organizing the flow of data on telecommunications lines.)

This manual is arranged in five sections. Section I describes the features of the 12966A and its specifications. Section II presents an overview of the principles of operation. Section III provides driver programming information. Section IV contains installation and checkout instructions. Section V contains component location, block, schematic, and timing diagrams.

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INTRODUCING THE HP 12966A

SECTION I

The HP 12966A Buffered Asynchronous Data Communications Interface is a hardware interface kit that provides half-duplex, asynchronous bit-serial data transfer between the CPU (HP 2116, HP 2100, or HP 1000 Computers) and asynchronous data sets or terminals which comply with Electronic Industries Association Standard RS-232-C.

You can program the interface kit to transfer data under direct memory access (this is called "dual channel port controller" in the HP 1000 Computers), interrupt, or skip-on-flag program control.

Note: The term "direct memory access" or "DMA" is used throughout this manual and includes the dual channel port controller (DCPC).

The interface kit operates in either character mode or buffer (page) mode. During receive operations (that is, data being sent from a device to the interface) the interface can operate in either mode. In character mode, the interface will interrupt or skip-on-flag every time that a character is received from the device. In buffer mode, the interface will accept up to 128 characters from a device and cause an interrupt or skip-on-flag condition depending upon the status of the buffer (empty, half-full, or full).

During transmit operations (that is, data being sent from the CPU to the interface) the interface operates in buffered mode. Up to 128 characters are received from the CPU and sent to the device at the programmed baud rate. Buffer status is indicated by an interrupt or skip-on-flag condition at buffer half-full, full, and empty. A detailed discussion of interface operation is presented in section II.

The interface provides parity (if selected), start, and stop bits to each character sent to the device. When data is received from the device, the interface strips these bits from each character so that only the character bits are sent to the CPU.

1-1. FEATURES

The features of the interface include:

- You can select one of 16 baud rates (from 50 to 9600 baud, including an externally-supplied X16 clock), either through your program or by hardwiring jumpers in the cable connector.
- You can select character length (5 to 8 bits) and number of stop bits (1 or 2) through your program. (When a 5-bit character length is selected, the number of stop bits that you can select is either 1 or 1½.)
- You can select parity (on/off) and parity sense (odd/even) through your program.
- 128 X 8-bit character buffering which allows the CPU to transfer data to/from the HP 12966A at a faster rate than the transfer rate between the HP 12966A and the I/O device.
- You can program the HP 12966A to recognize up to 256 different characters through program control of a 256 special character memory (RAM).
- Interrupt flags you can test for, indicating when the buffer is full, half-full, and empty, buffer overrun, break, and when a special character (that you have designated) has been received.
- Continuous monitoring of RS-232-C input lines to allow you to program the HP 12966A to interrupt when any of the lines that you select change state.
- A counter to indicate the number of characters in the buffer, which can be accessed through your program.

1-2. KIT CONTENTS

1-3. Standard Version

The standard interface kit provides connection to an HP 2600 or HP 2615 Terminal and contains the following items:

a. Buffered Asynchronous Data Set Printed Circuit Assembly (PCA), part no. 12966-60001.

b. Interconnecting Cable Assembly, 50 feet, part no. 12966-60004.

c. Test Connector, part no. 12966-60003.

d. This Reference Manual, part no. 12966-90001.

1-4. Option 001 (Direct Cable to HP 2640 Series Terminals)

Option 001 replaces the standard cable assembly with Interconnecting Cable Assembly, 50 feet, part no. 12966-60008. This cable interfaces the HP 264X Terminal.

1-5. Option 002 (Modem Cable)

Option 002 replaces the standard cable assembly with Interconnecting Cable Assembly, 50 feet, part no. 12966-60006. This cable interfaces the 103 and 202 Data Sets.

1-6. Option 003 (Direct Cable to HP 2749B)

Option 003 replaces the standard cable assembly with Interconnecting Cable Assembly, 25 feet, part no. 12966-60007. This cable interfaces the HP 2749B Teleprinter.

1-7. Option 004 (Direct Cable to HP 7221A and HP 264X)

Option 004 replaces the standard cable assembly with two interconnecting cable assemblies. One cable assembly, 50 feet, part no. 12966-60011. This cable interfaces the HP 7221A to the 12966A. The second cable assembly, 5 feet, part no. 12966-60012. This cable interconnects the plotter and a HP 264X Terminal.

1-8. Option 005 (Direct Cable to HP 2621)

Option 005 replaces the standard cable assembly with interconnecting cable assembly, 50 feet, part no. 12966-60010. This cable interfaces the HP 2621 Terminal.

1-9. SYSTEM CONFIGURATION

The interface printed circuit assembly (PCA) occupies one I/O slot and uses one I/O select code. An interface PCA is required for each communication channel. Two typical configurations are shown in figure 1-1. Connection to the computer is via the standard I/O bus. The interface PCA is driven by your coded software program which uses five control words and one data word to transfer infromation from the CPU to the interface PCA. Information transfer from the interface PCA to your program is achieved with one status word and one data word. The interface PCA is byte oriented, inputting or outputting one byte of data per I/O transfer (LIA/B, OTA/B instructions).

1-10. SPECIFICATIONS

Specifications for the 12966A are given in table 1-1.

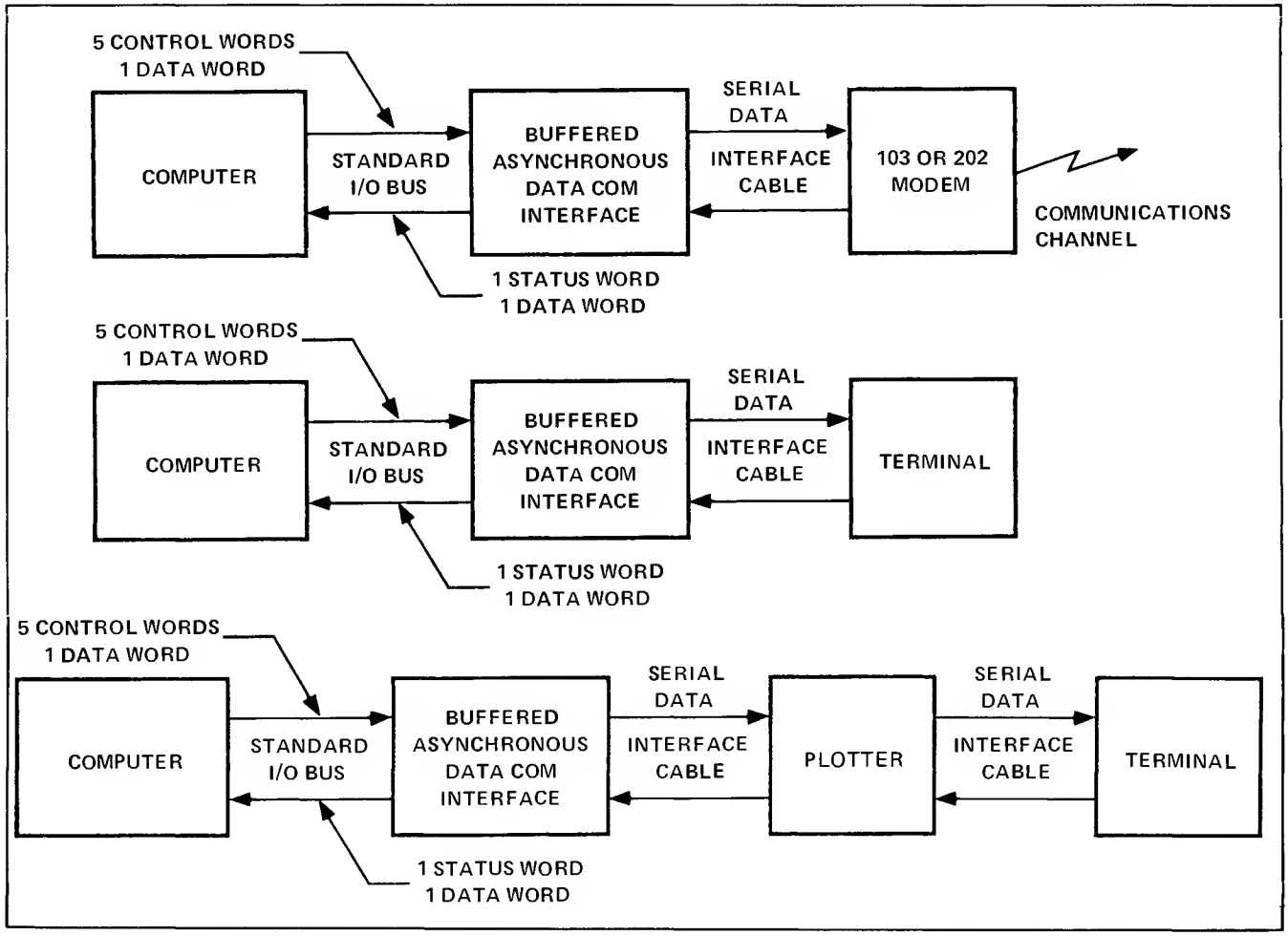


Figure 1-1. System Configurations Block Diagram

Table 1-1. Specifications

CHARACTERISTICS	SPECIFICATIONS
Function:	Asynchronous device operating in half duplex mode that converts parallel data to serial data for transmission and converts received serial data to parallel data.
Compatibility:	Standard Kit: Used with HP 2600 or HP 2615 Terminals. Option 001: Used with HP 264X Terminals. Option 002: Used with HP currently-supported Bell Telephone System 103 and 202 type data sets.

Table 1-1. Specifications (Continued)

CHARACTERISTICS	SPECIFICATIONS
	Option 003: Used with HP 2749B Teleprinter. Option 004: Used with HP 7221 Plotter and HP 264X Terminal. Option 005: Used with HP 2621 Terminals.
Interface Requirements:	Conforms to Electronic Industries Association Standard RS-232-C.
Data Transfer Rate to/from Data Set Modem:	Adjustable with program selection or hardware jumpers to discrete rates between 50 and 9600 baud. The rates are: 50 134.5 600 1800 4800 75 150 900 2400 7200 110 300 1200 3600 9600 An external X16 clock line can also be selected by your program or by hardware jumpers.
Character Size: (Input/Output of Computer)	Adjustable with program selection from five to eight bits.
Stop Bits:	Adjustable with program selection to either 1 or 2 (when six, seven, or eight character bits are selected). When five character bits are selected, the number of selectable stop bits is either 1 or 1½.
Parity:	Programmable selection of parity (on/off) and parity sense (odd/even).
Character Buffering:	128 X 8-bit buffer.
Special Characters:	256 special character memory. (You define the special characters by your program.)
Interrupt Flags:	Flag indication when: Buffer is full. Buffer is half full. Buffer is empty. Special character is received. Buffer Overrun/Parity Error. Break condition occurs. Device status line (CB, CC, CE, CF, SBB, or SCF) has changed state, if enabled by your program.
Power Consumption from Computer	
+5-volt supply:	1.95A nominal, 3A maximum
+12-volt supply:	18 mA nominal
-2-volt supply:	66 mA nominal, 100 mA maximum
-12-volt supply:	59 mA nominal

SECTION II

PRINCIPLES OF OPERATION

This section gives an overview of the principles of operation of the interface. The HP 12966A operates in either of two selectable modes; transmit or receive. Figure 2-1 shows the nine words used to transfer data and control the HP 12966A. These words are described in detail in section III, Programming.

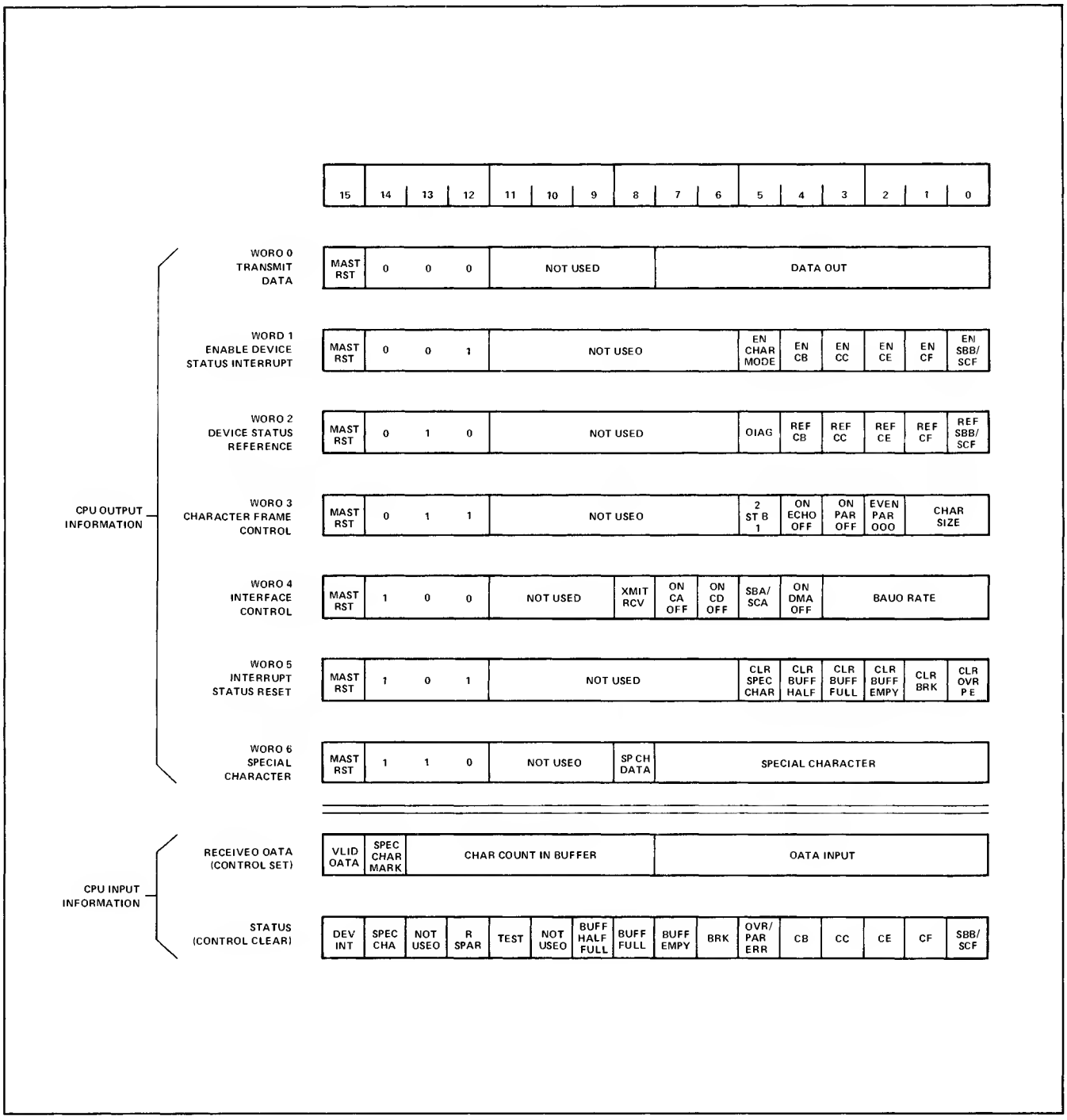


Figure 2-1. Data Transfer and Control Words

2-1. TRANSMIT MODE

The transmit mode is defined as the direction of data transfer from the CPU to a terminal, either directly or through a modem. All data to be transmitted originates in the CPU. (You should refer to figure 2-2 while reading the discussion of the transmit mode.)

Prior to transferring data to the interface PCA for transmission, you must configure the PCA for the correct character size, parity, stop bits, and baud rate. Control Words 3 and 4, which are described in section III, configure the PCA. Once the PCA has been correctly configured, data transfer can be initiated.

Data transfer between the CPU and the interface PCA occurs in the form of 8-bit parallel bytes. No unpacking by the PCA is provided, that is, data cannot be sent to the PCA in the form of two data bytes in a 16-bit word because the PCA has no provisions for separating the two bytes. Therefore, data must be transferred in the Word 0 format described in section III.

The data transfer may occur under program control (either interrupt or skip-on-flag) or direct memory access control. Each data byte from the CPU is entered into a 128 X 8-bit First-In-First-Out (FIFO) buffer memory on the PCA. Consequently it is possible to accept up to 128 data bytes from the CPU, regardless of the transmission baud rate. The output of the FIFO buffer is applied to a Universal Asynchronous Receiver/Transmitter (UART) which converts the parallel data into a serial word that contains the data along with start, parity, and stop bits. When parity is enabled, the UART automatically computes the parity of the specified sense (either odd or even) and adds it to the serial data transmission. As each data byte is transmitted, the next data byte is read out of the FIFO buffer and transmitted until the buffer is empty. The UART controls the baud rate which is selected by Control Word 4 when the PCA is configured. The Buffer Empty Status Flag is set after the last data byte in the buffer has been transmitted.

When transmitting data bytes from the CPU to the interface PCA, you do not have to issue STC and CLF instructions with each data byte transfer. The interface PCA sets the Buffer Half-Full Status Flag when 64 data bytes have been received from the CPU. Only one STC,C instruction is required to allow the flag to be set when the buffer is half-full. The flag will be set again when the buffer is full (128 bytes), provided that another STC,C instruction is issued and the Buffer Half-Full Status Flag is cleared. If a block of 128, or less, data bytes is transferred, the STC,C instruction may be issued after the data transfer to permit the Buffer Empty Status Flag to set when the buffer has been emptied.

2-2. RECEIVE MODE

The receive mode (see figure 2-3) is defined as the data transfer from a terminal, or modem, to the CPU. As in the transmit mode, you must configure the interface PCA for the correct character size, parity, stop bits, and baud rate. Control Words 3 and 4, which are described in section III, configure the PCA. Once the PCA is configured, data transfer can be initiated. The PCA does not need to be reconfigured each time the operating mode is changed if the character size, parity, stop bits, and baud rate are the same for both receive and transmit modes.

Data transfer between the PCA and the CPU occurs in the form of 8-bit parallel bytes. No packing by the PCA is provided, that is, data cannot be sent to the CPU in the form of two data bytes in a 16-bit word because the PCA has no provisions for combining the two 8-bit bytes. Therefore, data is transferred in the Received Data Word format described in section III.

The data transfer may be accomplished under either program control (interrupt or skip-on-flag) or direct memory access control. The serial data received by the PCA from the terminal, or modem, is transformed into a parallel byte by the receiving portion of the UART. If parity check is enabled, the UART calculates

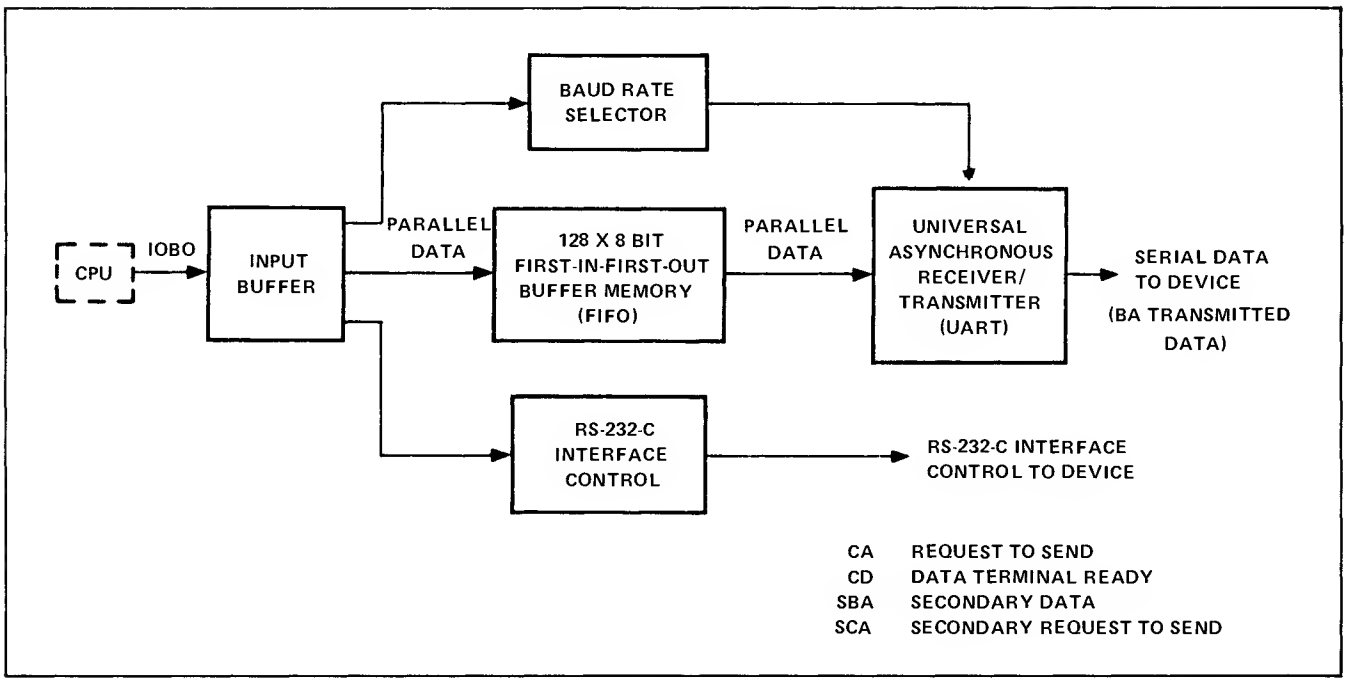


Figure 2-2. Transmit Mode Data Transfer

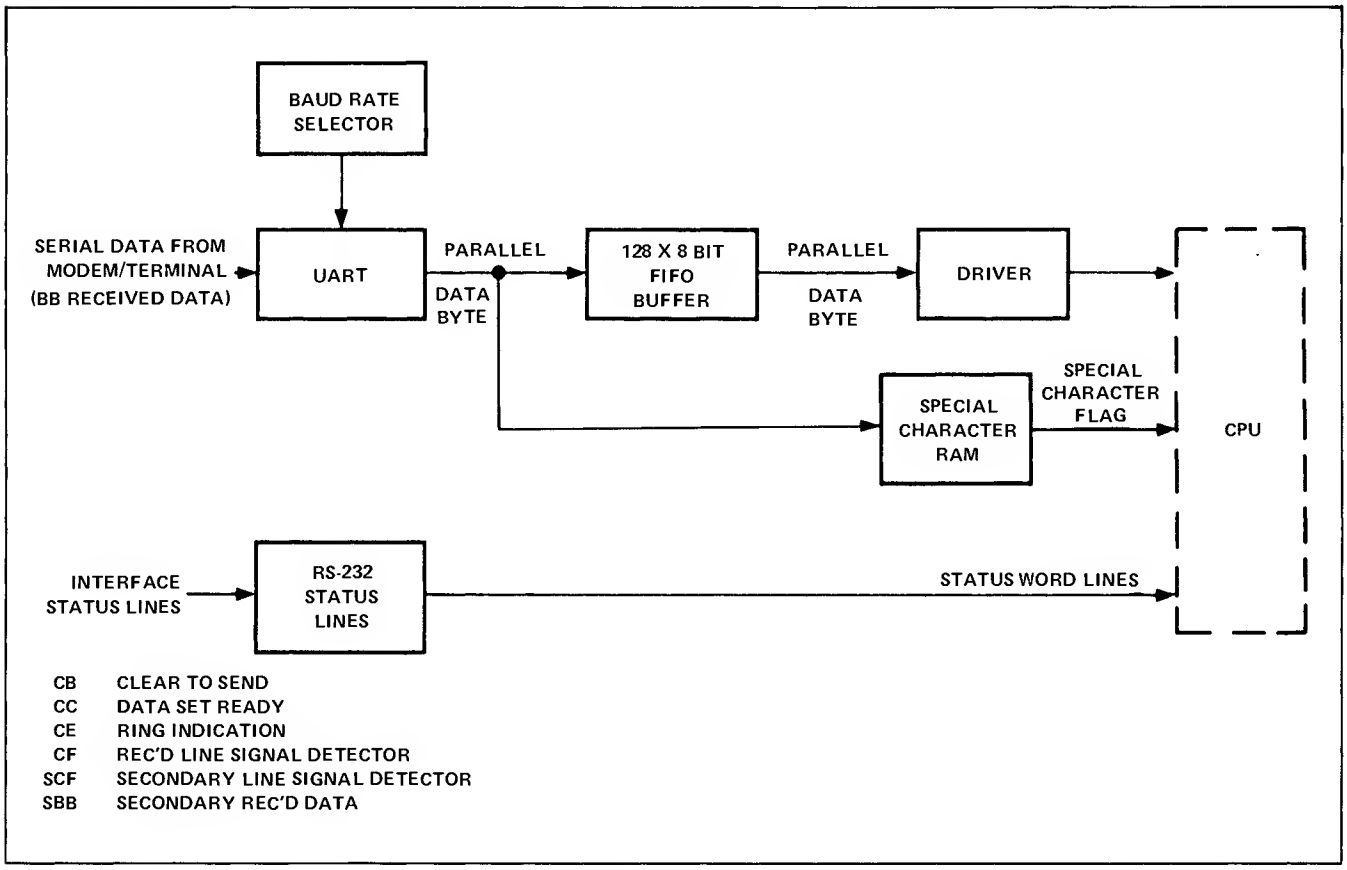


Figure 2-3. Receive Mode Data Transfer

the correct parity and compares it with the parity bit in the received character bit stream. If the calculated parity bit does not correlate with the received parity bit, a parity error is generated. Parity is stripped from the data byte and therefore is not available to the program. In addition to parity, the UART also tests for stop bits. The absence of stop bits and all zero data will result in a break condition.

After parity and stop tests, the parallel data byte from the UART is applied to the Special Character random access memory (RAM) to determine whether or not the received data byte is one you have designated as a Special Character. If it is, the Special Character Status Flag will be set.

The data byte is transferred to the FIFO buffer for temporary storage until input to the CPU is executed. When the buffer is half-full, and full, the corresponding Status Flag is set. The CPU reads a data byte out of the FIFO buffer each time an LIA/B instruction is executed with the Control FF set. It is not necessary to issue STC and CLF instructions for each transfer of a data byte. Each successive LIA/B instruction reads the next data byte in the buffer until the buffer is empty. After the last data byte is read from the FIFO buffer, the Buffer Empty Status Flag will be set.

2-3. CPU-DEVICE INTERFACE DESCRIPTION

2-4. CPU Interface

The HP 12966A interfaces with the CPU via the I/O bus. You use standard I/O instructions to transfer information and control the interrupt protocol. Specific effects of each I/O instruction are discussed in section III, Programming.

Information transferred between the CPU and the buffered asynchronous data communications interface is:

a. Commands and Transmit Data from the CPU to the interface.

b. Status and Receive Data from the interface to the CPU.

Commands, transmit data, and receive data may be transferred under direct program control or direct memory access control. Status may be transferred under direct program control only. It is received with every LIA/B instruction whenever the Control FF is clear.

2-5. Device Interface

The HP 12966A-to-device interface consists of two data transfer lines, four modem/terminal control lines, and six modem/terminal status lines.

The two data transfer lines are:

a. Transmitted Data (BA)

b. Received Data (BB)

The four modem/terminal control lines are:

a. Request to Send (CA)

b. Data Terminal Ready (CD)

c. Secondary Data (SBA)

d. Secondary Request to Send (SCA)

These lines, further defined in RS-232-C, are under program control. Only three of the four are used at any one time (CA, CD, and SBA or SCA), as dictated by hardware jumpers on the cable connector. (Refer to tables 4-2 through 4-8.)

The six modem/terminal status lines are:

a. Clear to Send (CB)

b. Data Set Ready (CC)

c. Ring Indication (CE)

d. Received Line Signal Detector (CF)

e. Secondary Line Signal Detector (SCF)

f. Secondary Received Data (SBB)

Five of the six status lines (CB, CC, CE, CF, and either SCF or SBB) from the modem/terminal are forwarded to your program in the Status Word. Also, the HP 12966A monitors these status lines to generate an interrupt if a change occurs. This interrupt capability is controlled by two commands (Control Words 1 and 2, which are defined in section III) which enable or disable interrupts from each status line, and which define what line sense should cause an interrupt to occur.

SECTION III

PROGRAMMING

This section provides you with the information necessary to code your driver program. Software interface characteristics are discussed first, followed by an explanation of various words used to control the PCA. A sample program flowchart and listing are given at the end of the section.

3-1. SOFTWARE INTERFACE CHARACTERISTICS

The HP 12966A Buffered Asynchronous Data Communications Interface follows the standard software protocol with a few exceptions:

a. STC,C is not required to initiate a character transfer.

b. STC is required to enable status interrupts (buffer full, buffer empty, etc.).

c. The Status Flags are always set for the following conditions when under direct memory access or program control:

DIRECT MEMORY ACCESS CONTROL		PROGRAM CONTROL	
TRANSMIT MODE	RECEIVE MODE	TRANSMIT MODE	RECEIVE MODE
Device Status Line Change	Device Status Line Change	Device Status Line Change	Device Status Line Change
	Break	Buffer Empty	Break
	Buffer Overrun	Buffer Half-Full	Buffer Overrun
	Parity Error	Buffer Full	Parity Error
	Special Character		Special Character
			Buffer Empty
			Buffer Half-Full
			Buffer Full

d. The Flag is not set on completion of a character output to the device or Input from the device.

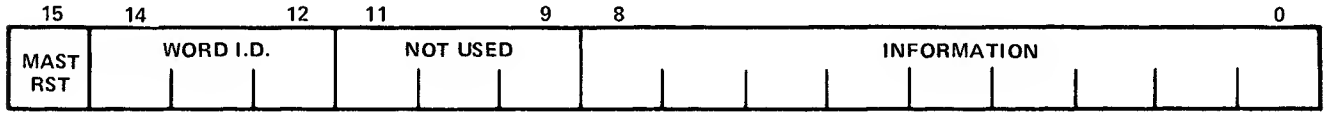
e. When operating under direct memory access control, a Service Request (SRQ) is generated whenever a data character is ready for input or output, providing that an interrupt condition listed in "c" above is not pending. The Flag and SRQ functions are separated to permit interrupts to pass through during a direct memory access data transfer.

f. The interface is controlled with six output words and two input words.

3-2. WORD FORMATS

3-3. CPU Output Word Format

Information transfer from the CPU to the HP 12966A is implemented by six different words (five command words and one data word) in the following general format. The "information" and "not used" field lengths vary, depending upon the word type.

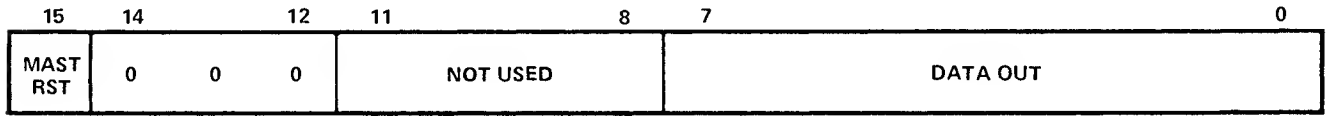


Bit 15 in all information transfers from the CPU to the HP 12966A is designated the Master Reset bit. This means that any OTA/B instructions to the interface with a "1" in bit 15 will result in a Master Reset which is described in detail later in this section. The Master Reset function is executed first, followed by transfer of the information part of the word (bits 0—8) to the designated destination. If, for example, word 4 is transferred to the interface with bit 15 a "1", the interface is reset first, then the baud rate, modem control bits, etc, are shifted into the correct registers. The Master Reset function is not recommended when coding the Transmit Data Word (Word 0).

Each command and data word is discussed in the following paragraphs.

3-4. Transmit Data Word (Word 0)

Word 0 is used to transfer one data byte from the CPU to the interface for transmission to the modem or terminal. The format of Word 0 is as follows:



Transmit Data Word (Word 0)

BIT	DESIGNATION	DESCRIPTION
0 - 7	Data Byte	Data byte to be transmitted to modem or terminal.
12 - 14	Word Type	All three bits are "0"s to designate the Transmit Data Word (word 0).
15	Master Reset	"0" = do not execute a master reset. "1" = execute a master reset. Note: Using Master Reset in Word 0 is not recommended; therefore, code "0" for bit 15.

3-5. Enable Device Status Interrupt Word (Word 1)

Word 1 enables, or disables, the interface to generate an interrupt whenever a device status line changes to a signal state different from that referenced in the Device Status Reference Word (Word 2). The format of Word 1 is as follows:

15	14		12	11	6	5	4	3	2	1	0
MAST RST	0	0	1	NOT USED		EN CHAR MODE	EN CB	EN CC	EN CE	EN CF	EN SBB/ SCF

Enable Device Status Interrupt Word (Word 1)

BIT	DESIGNATION	DESCRIPTION
0	Enable SBB/SCF	"0" = do not generate an interrupt if the Secondary Receive Data line or the Secondary Received Line Signal Detector line changes state. "1" = generate an interrupt if the Secondary Receive Data line or the Secondary Received Line Signal Detector line changes state.
1	Enable CF	"0" = do not generate an interrupt if the Receive Line Signal Detector line changes state. "1" = generate an interrupt if the Receive Line Signal Detector line changes state.
2	Enable CE	"0" = do not generate an interrupt if the Ring Indicator line changes state. "1" = generate an interrupt if the Ring Indicator line changes state.
3	Enable CC	"0" = do not generate an interrupt if the Data Set Ready line changes state. "1" = generate an interrupt if the Data Set Ready line changes state.
4	Enable CB	"0" = do not generate an interrupt if the Clear to Send line changes state. "1" = generate an interrupt if the Clear to Send line changes state.
5	Enable Character Mode	"0" = do not operate in character mode. The Flag will be set only when the buffer is half-full, buffer is full, or special character. "1" = operate in character mode. The Flag will be set whenever a valid character is present at the output of the buffer in receive mode.
12 - 14	Word Type	Bits are set to an octal "1" to designate the Enable Device Status Interrupt Word (Word 1).
15	Master Reset	"0" = do not execute a master reset. "1" = execute a master reset.

3-6. Device Status Reference Word (Word 2)

Word 2 sets up the reference state to which the corresponding device status input lines are compared. If any of the status lines differ from the reference and it has been enabled by the Enable Device Status Interrupt Word (Word 1), an interrupt is generated. The format of Word 2 is as follows:

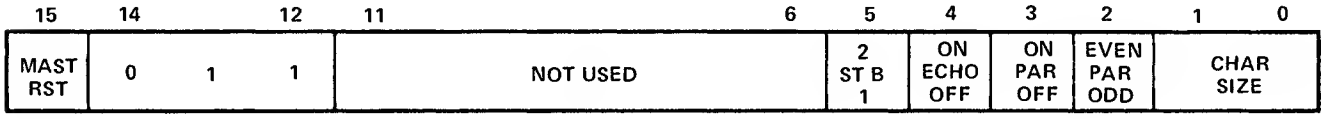
15	14	13	12	11 ... 6	5	4	3	2	1	0
MAST RST	0	1	0	NOT USED	DIAG	REF CB	REF CC	REF CE	REF CF	REF SBB/ SCF

Device Status Reference Word (Word 2)

BIT	DESIGNATION	DESCRIPTION
0	Reference SBB/SCF	SBB (Secondary Received Data): "0" = binary "0" data. "1" = binary "1" data. SCF (Secondary Received Line Signal Detector): "0" = ON "1" = OFF.
1	Reference CF	"0" = Received Line Signal Detector ON. "1" = Received Line Signal Detector OFF.
2	Reference CE	"0" = Ring Indicator ON. "1" = Ring Indicator OFF.
3	Reference CC	"0" = Data Set Ready ON. "1" = Data Set Ready OFF.
4	Reference CB	"0" = Clear to Send ON. "1" = Clear to Send OFF.
5	Diagnostic	This bit is available at the interface connector for diagnostic test purposes.
12 - 14	Word Type	Bits are set to an octal "2" to designate the Device Status Reference Word (Word 2).
15	Master Reset	"0" = do not execute a master reset. "1" = execute a master reset.

3-7. Character Frame Control Word (Word 3)

Word 3, except for the ECHO bit, controls the operation of the Universal Asynchronous Receiver/ Transmitter (UART) by specifying the character size, number of stop bits, and parity. The ECHO bit enables the echo function when the interface is in the receive mode. The format of Word 3 is as follows:



Character Frame Control Word (Word 3)

BIT	DESIGNATION	DESCRIPTION
0-1	Character Size	Bit Field (1 0) / Number of Bits/Character (Not Including Parity): 0 0 = 5; 0 1 = 6; 1 0 = 7; 1 1 = 8
2	Parity Odd/Even	"0" = odd parity. "1" = even parity.
3	Parity On/Off	"0" = parity generator/checker is OFF. "1" = parity generator/checker is ON.
4	Echo On/Off	"0" = echo is OFF "1" = echo is ON.
5	Number of Stop Bits	"0" = one stop bit. "1" = two stop bits. (One and one-half stop bits when 5 character bits are selected.)
12 - 14	Word Type	Bits are set to an octal "3" to designate Character Frame Control Word (Word 3).
15	Master Reset	"0" = do not execute a master reset. "1" = execute a master reset.

3-8. Interface Control Word (Word 4)

Word 4 controls the RS-232-C output control lines, defines the baud rate, identifies the upcoming DMA transfer, and places the interface in either transmit or receive mode. The format of Word 4 is as follows:

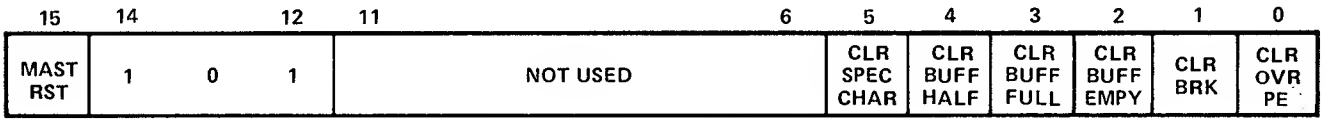
15	14		12	11 9	8	7	6	5	4	3 0
MAST RST	1	0	0	NOT USED	XMIT RCV	ON CA OFF	ON CD OFF	SBA/ SCA	ON DMA OFF	BAUD RATE

Interface Control Word (Word 4)

BIT	DESIGNATION	DESCRIPTION
0 - 3	Baud Rate	Bit Field (3 2 1 0) / Baud Rate: 0 0 0 0 — External Clock (X16) 0 0 0 1 — 50 0 0 1 0 — 75 0 0 1 1 — 110 0 1 0 0 — 134.5 0 1 0 1 — 150 0 1 1 0 — 300 0 1 1 1 — 600 1 0 0 0 — 900 1 0 0 1 — 1200 1 0 1 0 — 1800 1 0 1 1 — 2400 1 1 0 0 — 3600 1 1 0 1 — 4800 1 1 1 0 — 7200 1 1 1 1 — 9600
4	DMA (Direct Memory Access)	"0" = program control data transfer. "1" = DMA control data transfer.
5	SBA/SCA	SBA (Secondary Transmit Data): "0" = binary "0" data. "1" = binary "1" data. SCA (Secondary Request to Send): "0" = OFF. "1" = ON.
6	CD	"0" = Data Terminal Ready OFF. "1" = Data Terminal Ready ON.
7	CA	"0" = Request to Send OFF. "1" = Request to Send ON.
8	Transmit/Receive	"0" = receive mode. "1" = transmit mode.
12 - 14	Word Type	Bits are set to an octal "4" to designate the Interface Control Word (Word 4).
15	Master Reset	"0" = do not execute master reset. "1" = execute master reset.

3-9. Interrupt Status Reset Word (Word 5)

Word 5 permits the software driver to individually clear the source(s) of an interrupt. Once a condition on the interface results in an interrupt, the interrupt will remain until it is cleared by a specific bit in Word 5, even if the causal condition may no longer be present. The format of Word 5 is as follows:



Interrupt Status Reset Word (Word 5)

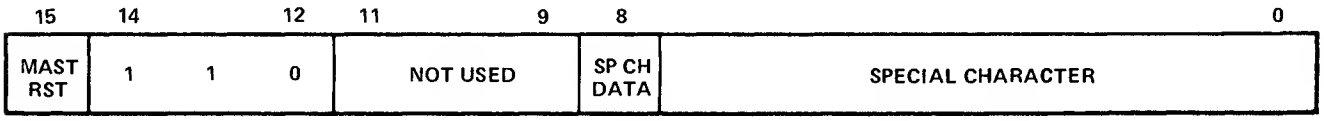
BIT	DESIGNATION	DESCRIPTION
0	Clear Overrun/Parity Error Status Flag	"0" = do not clear the flag. "1" = clear the flag.
1	Clear Break Status Flag	"0" = do not clear the flag. "1" = clear the flag.
2	Clear Buffer Empty Status Flag	"0" = do not clear the flag. "1" = clear the flag.
3	Clear Buffer Full Status Flag	"0" = do not clear the flag. "1" = clear the flag.
4	Clear Buffer Half-Full Status Flag	"0" = do not clear the flag. "1" = clear the flag.
5	Clear Special Character Status Flag	"0" = do not clear the flag. "1" = clear the flag.
12 - 14	Word Type	Bits are set to octal "5" to specify the Interrupt Status Reset Word (Word 5).
15	Master Reset	"0" = do not execute master reset. "1" = execute master reset.

3-10. Special Character Word (Word 6)

Word 6 adds or removes the designated character from the special character list. If a designated special character is received while the interface is in the receive mode, an interrupt is generated. The card must be in Transmit Mode to alter the contents of the Special Character RAM.

Note: Every character must be either cleared or identified as a special character at interface initialization.

The format of Word 6 is as follows:



Special Character Word (Word 6)

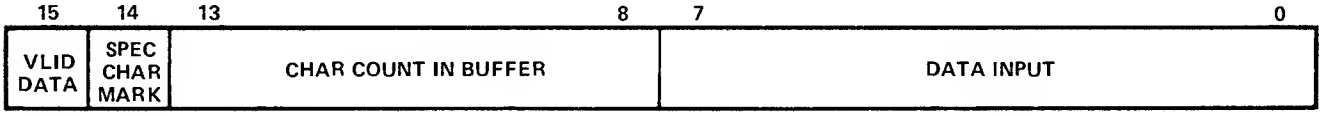
BIT	DESIGNATION	DESCRIPTION
0 - 7	Special Character	This is the character which is to be added, or removed, from the special character list.
8	Special Character Data	"0" = the character in bits 0 thru 7 is not a special character; remove from list. "1" = the character in bits 0 thru 7 is a special character; add to list.
12 - 14	Word Type	Bits are set to an octal "6" to specify the Special Character Word (Word 6).
15	Master Reset	"0" = do not execute master reset. "1" = execute master reset.

3-11. CPU Input Word Format

Information transfer from the interface to the CPU is implemented with two words. The Received Data Word is available whenever the Control FF is set, and the Status Word is available whenever the Control FF is clear. The interface formats these two words, and the formats are described below.

3-12. Received Data Word (Control Set)

The Received Data Word is available to the CPU when the Control FF is set. This word contains a character/data byte (up to 8 bits), a special character mark bit, a valid data bit, and a 6-bit binary character count indicating the number of data bytes currently in the buffer.



Received Data Word

BIT	DESIGNATION	DESCRIPTION
0 - 7	Received Data	Up to 8-bit data byte received from the modem or terminal.
8 - 13	Character Count	The character count indicates the number of characters in the buffer, including the character in bits 0 thru 7 of this word. The meanings of the various counts are shown below: Count: $00_8 \downarrow 77_8$ — Meaning: Empty Count: $00_8 \downarrow 77_8$ — Meaning: or Half-Full Count: $100_8 \downarrow 177_8$ — Meaning: or Full Count: 200_8 — Meaning: or Full
14	Special Character Marker	"0" = the character/data byte in bits 0 thru 7 is not a special character. "1" = the character/data byte in bits 0 thru 7 is a special character.
15	Valid Data Marker	"0" = the character/data byte in bits 0 thru 7 is not a valid character/data byte. "1" = the character/data byte in bits 0 thru 7 is a valid character/data byte.

3-13. Status Word (Control Clear)

The Status Word is input when the Control FF is clear. This word contains the real-time modem/terminal status lines which do not have to be cleared. In addition to the status lines, the word contains flags which identify the cause of the interrupt. These flags must be cleared since they may not represent current status. The format of the Status Word is described below.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DEV INT	SPEC CHA	NOT USED	R SPAR	TEST	NOT USED	BUFF HALF FULL	BUFF FULL	BUFF EMPY	BRK	OVR/ PAR ERR	CB	CC	CE	CF	SBB/ SCF

Status Word

BIT	DESIGNATION	DESCRIPTION
0	SBB/SCF	SBB (Secondary Received Data): "0" = binary "0" data. "1" = binary "1" data. SCF (Secondary Received Line Signal Detector): "0" = OFF. "1" = ON.
1	CF	"0" = Received Line Signal Detector OFF. "1" = Received Line Signal Detector ON.
2	CE	"0" = Ring Indicator OFF. "1" = Ring Indicator ON.
3	CC	"0" = Data Set Ready OFF. "1" = Data Set Ready ON.
4	CB	"0" = Clear to Send OFF. "1" = Clear to Send ON.
5	Overrun or Parity Error	"0" = no parity error or data buffer overrun. "1" = parity error or data buffer overrun.
6	Break	"0" = no break conditions present. "1" = break condition has been detected and has been terminated.
7	Buffer Empty	"0" = buffer is not empty. "1" = buffer is empty.

Status Word (Continued)

BIT	DESIGNATION	DESCRIPTION
8	Buffer Full	"0" = buffer is not full. "1" = buffer is full.
9	Buffer Half-Full	"0" = buffer is not half-full. "1" = buffer is half-full. This flag is set only as the buffer is filling up and reaches (and exceeds) half-full status. The flag is not set as the buffer reaches (and drops below) half-full status as it is being emptied.
11	Test	This bit represents the unprocessed received serial data line (BB), and is used for diagnostic purposes.
12	Spare Receiver Input	This bit is the output of a spare RS-232-C line receiver which is available through the device interface connector (P1-U of the interface cable).
14	Special Character	"0" = no special character has been received. "1" = a special character has been received.
15	Device Interrupt	"0" = no device status line interrupt. "1" = a device status line (CB, CC, CE, CF, and SBB/SCF in bit field 0 thru 4 of this word) that has been enabled, has changed and is causing an interrupt.

3-14. EFFECTS OF I/O INSTRUCTIONS

3-15. Master Reset

Master Reset is generated as a result of various I/O instructions or functions:

a. At power ON, or a front panel PRESET.

b. Issuing a CLC 0 instruction.

c. Bit 15 being a "1" in any of the information words transferred from the CPU to the interface (Word 0 through Word 6, which are described earlier in this section).

Master Reset places the interface in a known operating state as follows:

a. Receive operating mode.

b. Echo: OFF.

c. DMA: OFF.

d. Request to Send (CA): OFF

e. Data Terminal Ready (CD): OFF

f. Clears all data in the FIFO buffer.

g. Clears the Universal Asynchronous Receiver/Transmitter (UART); aborts transmission of any character immediately.

h. Clears the character counter.

i. Clears Service Request (SRQ).

j. Clears Control FF.

k. Sets Flag.

l. Sets Lockout (inhibits any conditions on the interface to generate an interrupt).

m. Clears the Device Status Interrupt Enable register thereby inhibiting any interrupt as a result of modem/terminal status change.

n. Special character list is *not* altered.

o. The following status flags are *not* affected: buffer empty, buffer half-full, buffer full, buffer overrun, special character, break, and parity error.

p. The character size, number of stop bits, parity, and parity sense are *not* altered.

q. The baud rate is *not* affected.

r. Clears out character mode enable for "Data Request Flag" which puts the interface back in buffered mode.

s. Clears the device reference register.

3-16. Set Control (STC) Instruction

STC enables interrupts from the interface, as with other 2100 Series Computer interfaces. But it also has two other important effects.

First, STC must be issued after the end of the service routine for each interface request (data or status), whether or not interrupts are being used. This is because of the interrupt interlock used by the interface to prevent interrupts occuring within interrupts (i.e., nested interrupts). In effect, the STC at the end of the service routine informs the interface that the current request has been serviced and that the program is ready to accept another request from the interface. Until the STC occurs, the interface will *not* be able to set its Flag to request further service.

If it is necessary to operate the interface in an interrupt environment, but not using the interrupt method for servicing the interface (i.e., interrupt system is on, but the interface is using "skip-on-flag" method of servicing), "false" interrupts can be prevented by following the STC immediately with the Clear Control (CLC) instruction.

Secondly, the STC is issued prior to requesting Received Data words. The Control FF must be set in order to input the data words.

3-17. Clear Control (CLC) Instruction

The CLC instruction is used to disable interrupts from the interface, as with other 2100 Series Computer interfaces. But it also affects the operation of the input word selector in the opposite manner as does the STC instruction. The Control FF must be clear in order to input the Status word.

> Note: Because of the interrupt interlock on the interface, it is not necessary to "clear control" following an interrupt; once an interrupt has occurred, no more interrupts can occur until an STC is issued. However, the CLC may be used for conformance with standard programming technique with no adverse effects.

3-18. Output A(OTA) Instruction

The OTA instruction is used to transfer information (CPU output Words 0 through 6) from the CPU to the interface. Word outputs with bit 15 set to a "1" are interpreted as Master Reset by the interface.

3-19. Load Into A (LIA) Instruction

The LIA instruction is used to transfer information (the Received Data and Status Words) from the interface to the CPU. Because the interface uses two types of input information (received data and status), the program and the interface must be able to know which type is to be supplied for any particular transfer. The selection is controlled by the program through the STC and CLC instruction.

3-20. SAMPLE PROGRAM

The sample program (see figures 3-1 and 3-2) demonstrates basic programming techniques for using the HP 12966A Buffered Asynchronous Data Communications Interface. This program can be used by the user as a test program to get started before writing his own program.

The user enters 64 characters from a remote terminal (an HP 2640A, or equivalent). These 64 characters are loaded into the FIFO buffer of the interface. When the Buffer Half-Full Status Flag is set, the data is transferred to a CPU buffer. The interface is then placed in the transmit mode, and the 64 characters are loaded back into the FIFO buffer from the CPU buffer. After the data is transferred, the interface transmits the characters in the FIFO buffer to the terminal.

Data transfer to/from the terminal is at 1200 Baud, one stop bit, eight-bit ASCII, no parity, and Echo is on. The program assumes that the interface PCA is in select code 12_8; however, this can be changed easily in the program to fit the user's equipment configuration.

> Note: To run the sample program of figure 3-2 it may be necessary to change the switch on your Data Communications PCA. All switches on the 02640-60089 or 02640-60143 should be set to OPEN except for A9, A10, and A11 on switch block S4 these should be CLOSED.

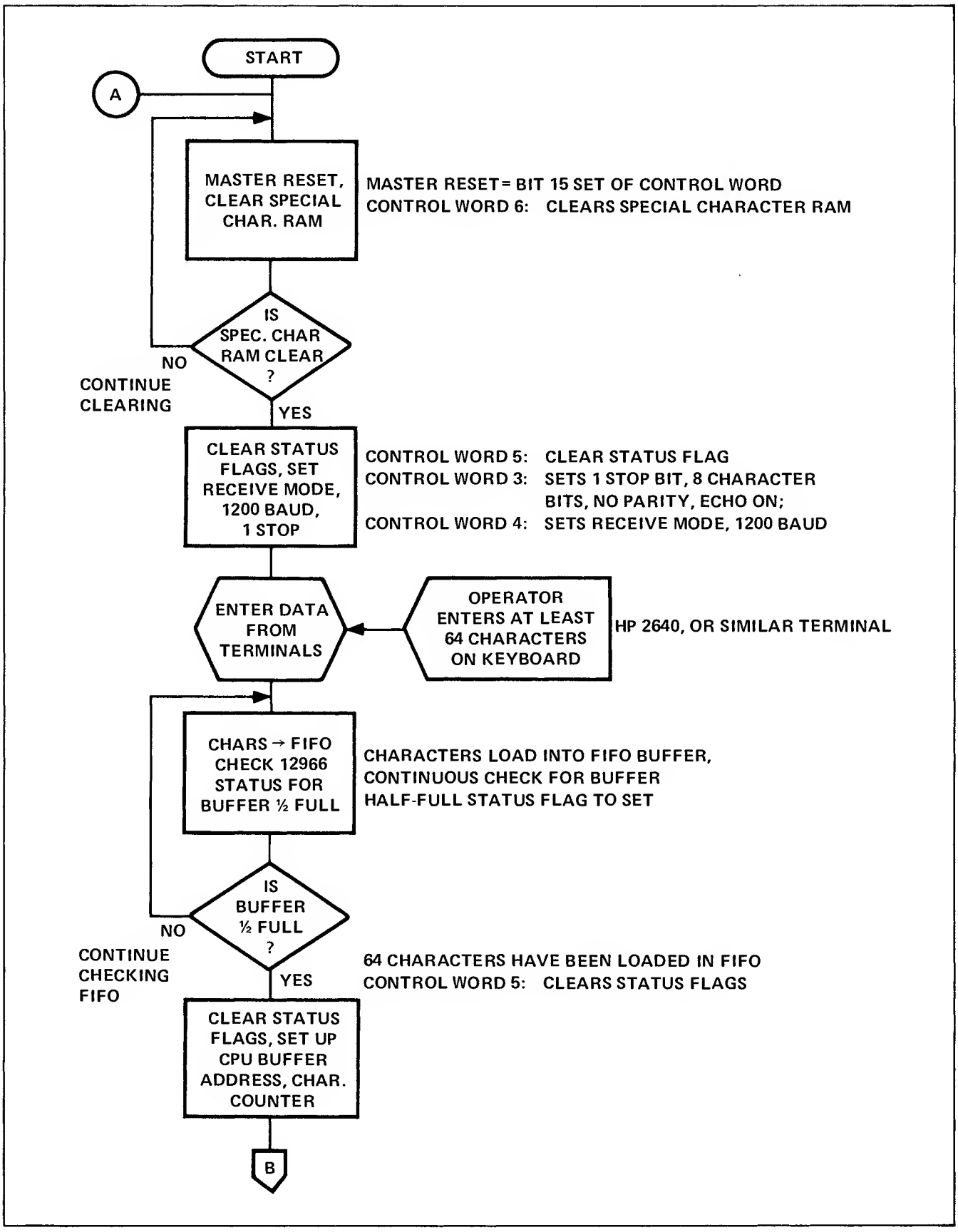


Figure 3-1. Sample Program Flowchart (Sheet 1 of 3)

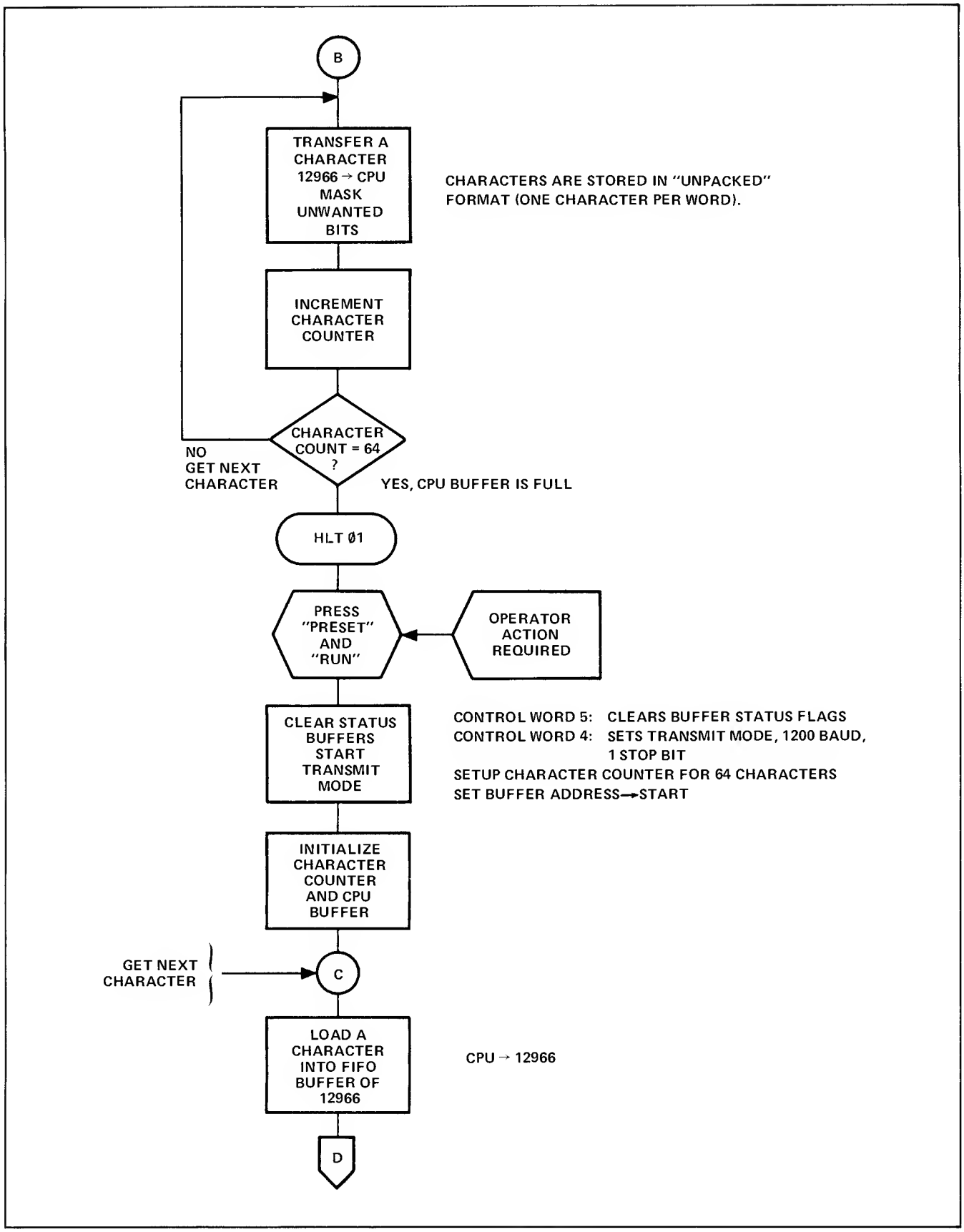


Figure 3-1. Sample Program Flowchart (Sheet 2 of 3)

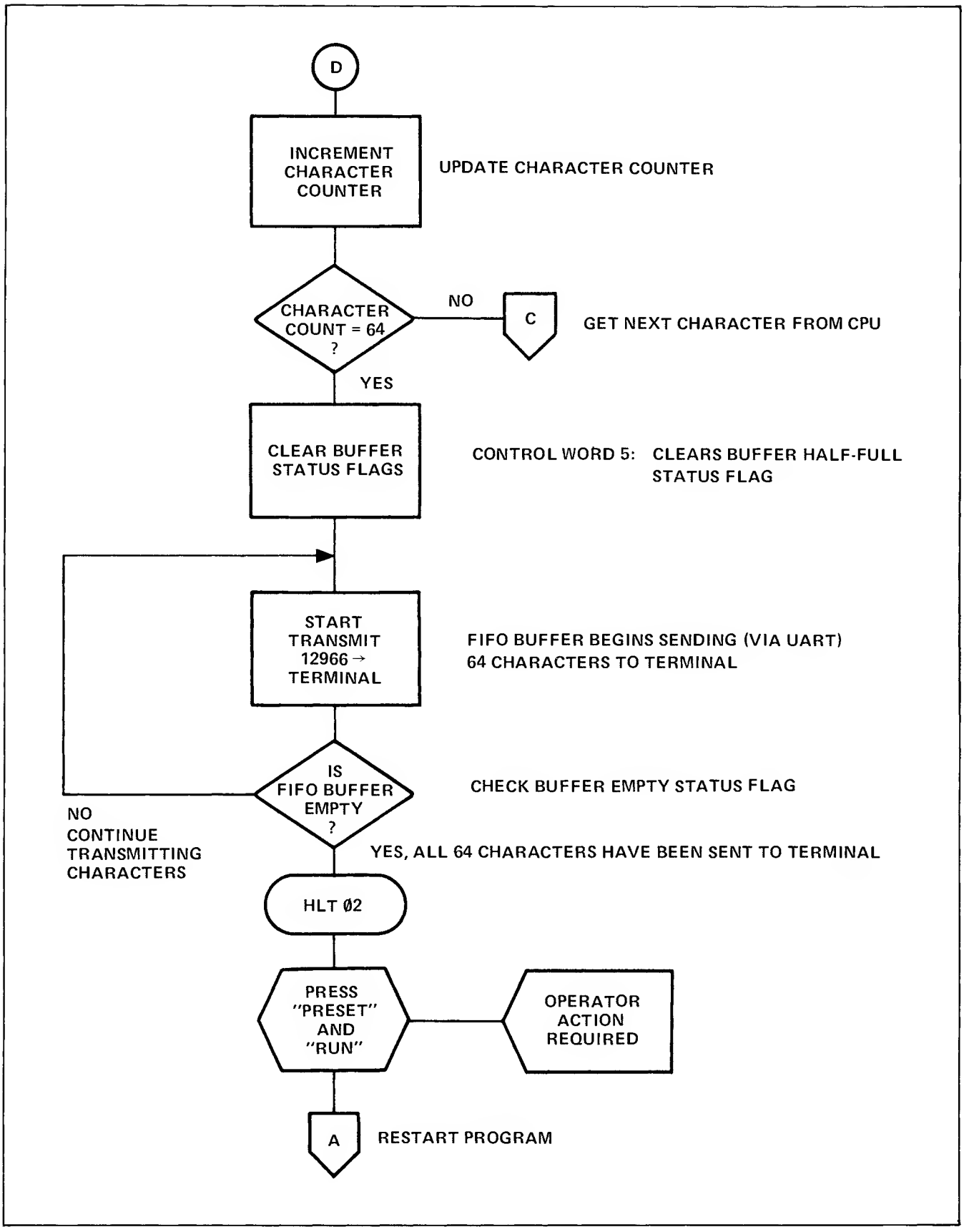


Figure 3-1. Sample Program Flowchart (Sheet 3 of 3)

```
0001  ASMB,A,B,L,T
0002        ORG 100B
0003  *
0004  ****12966 SAMPLE PROGRAM**************************
0005  *THE PROGRAM BEGINS BY CLEARING ALL ADDRESSES OF THE
0006  *SPECIAL CHARACTER RAM TO ZEROS.THE 12966 THEN IS
0007  *ENABLED TO RECEIVE MODE,1200 BAUD.THE USER ENTERS A
0008  *MINIMUM OF 64 CHARACTERS FROM THE TERMINAL KEYBOARD
0009  *(HP2640 OR SIMILAR TERMINAL). WHEN BUFFER HALF FULL
0010  *(64 CHARS.) IS DETECTED,THE CHARS. ARE TRANSFER FROM
0011  *THE FIFO BUFFER OF THE 12966 TO THE CPU. WHEN THIS
0012  *TRANSFER IS COMPLETED THE CPU HALTS (HLT 01).THE USER
0013  *PRESSES 'PRESET' & 'RUN', THE 12966 GOES INTO THE
0014  *TRANSMIT MODE. THE CPU BUFFER (64 CHARS.) IS SENT TO
0015  *THE 12966 FIFO BUFFER. WHEN THIS TRANSFER IS COMPLETED
0016  *THE 12966 TRANSMITS TO THE TERMINAL UNTIL BUFFER EMPTY
0017  *STATUS FLAG SETS. THE CPU NOW HALTS (HLT 02),PRESSING
0018  *'RUN' RESTARTS THE PROGRAM.
0019  *
0020  *
0021  A     EQU 0
0022  B     EQU 1
0023  SCT   EQU 12B       12966 IS IN SELECT CODE 12B
0024  SAVA  BSS 1
0025  SAVB  BSS 1
0026  COUNT BSS 1
0027  SIZE  DEC 64        64 CHARACTERS
0028  BHF   OCT 1000
0029  CW3   OCT 030023
0030  CW4R  OCT 040011
0031  CW4T  OCT 140411
0032  CW5   OCT 050077
0033  CW6   OCT 060000
0034  PAT   OCT 777
0035  DAB.  DEF DAB
0036  CLEAR OCT 060400
0037        ORG 1000B
0038  DAB   BSS 400
0039  *
0040  *
0041        ORG 200B
0042  START LDA CW4T      MASTER RESET,INITIALIZE TRANSMIT
0043        OTA SCT
0044        LDA CW6       CLEAR OUT SPECIAL CHAR RAM
0045  RI    OTA SCT
0046        INA
0047        CPA CLEAR     CHECK IF SPECIAL CHAR RAM IS CLEAR
0048        RSS           YES IT IS,CONTINUE WITH PROGRAM
0049        JMP RI        NO IT ISN'T,CONTINUE CLEARING
0050  OVER  LDA SIZE      SETUP AND INITIALIZE CHAR COUNTER
0051        CMA,INA       2'S COMP.
0052        STA COUNT
```

Figure 3-2. Sample Program Listing (Sheet 1 of 2)

```
0053          LDA CW5       LOAD WORD 5,CLEAR FLAGS
0054          OTA SCT
0055          LDA CW3       LOAD WORD 3,1 STOP BIT,8 DATA BITS
0056          OTA SCT         ECHO ON,NO PARITY
0057          LDA CW4R      LOAD WORD 4,RECEIVE MODE,1200 BAUD
0058          OTA SCT
0059  CHECK   STC SCT,C     SET CONTROL 12966
0060          SFS SCT       CHECK IF STATUS FLAG IS SET
0061          JMP *-1       NO,NONE IS SET,CONTINUE
0062          CLC SCT       YES,FLAG HAS SET
0063          LIA SCT       GET STATUS WORD
0064          AND BHF       CHECK FOR BUFFER HALF FULL
0065          SZA,RSS
0066          JMP CHECK     BHF NOT SET AS YET
0067          LDA CW5       BHF SET,CLEAR STATUS FLAGS
0068          OTA SCT
0069          LDB DAB.      SETUP CPU BUFFER ADDRESS
0070          STC SCT,C     SET CONTROL 12966
0071  T1      LIA SCT       GET A CHARACTER FROM FIFO
0072          AND PAT       MASK OUT UNWANTED BITS
0073          STA B,I       STORE CHAR INTO CPU BUFFER
0074          INB
0075          ISZ COUNT     INCREMENT COUNT,COUNT=64?
0076          JMP T1        NO,GET NEXT CHARACTER
0077          HLT 01        YES,CPU BUFFER IS FULL
0078  ***PRESS 'PRESET' AND 'RUN' TO PUT 12966 INTO TRANSMIT
0079  *MODE.
0080  *
0081          NOP
0082          LDA CW4T      SETUP 12966 TO TRANSMIT @1200 BAUD
0083          OTA SCT
0084          LDA CW5       CLEAR BUFFERS
0085          OTA SCT
0086          LDA SIZE      SETUP CHAR COUNTER
0087          CMA,INA       2'S COMP.
0088          STA COUNT
0089          LDB DAB.      SETUP BUFFER ADDRESS
0090          STC SCT,C
0091  T2      LDA B,I       GET A CHARACTER
0092          OTA SCT       PUT IT IN THE FIFO BUFFER
0093          INB
0094          ISZ COUNT     INCREMENT COUNT,COUNT=64?
0095          JMP T2        NO GET NEXT CHAR!!!
0096          LDA CW5       YES,LOAD W TO CLEAR BUFF
0097          OTA SCT           HALF FULL
0098          STC SCT,C   SET CONTROL,START TRANSMIT
0099          SFS SCT       IS BUFFER EMPTY?
0100          JMP *-1       NO,CONTINUE SENDING
0101          HLT 02        YES,IT IS EMPTY,HALT CPU!!
0102          JMP START     RESTART 12966
0103          END
```

Figure 3-2. Sample Program Listing (Sheet 2 of 2)

INSTALLATION AND SERVICING

SECTION IV

4-1. UNPACKING AND INSPECTION

If the shipping carton is damaged upon receipt, request that the carrier's agent be present when the kit is unpacked. Inspect the kit for damage (cracks, broken parts, etc.). If the kit is damaged and fails to meet specifications, notify the carrier and the nearest HP Sales and Service Office immediately. (Sales and Service Offices are listed at the back of this manual.) Retain the shipping container and the packing material for the carrier's inspection. The HP Sales and Service Office will arrange for the repair or replacement of the damaged kit without waiting for any claims against the carrier to be settled.

4-2. PREPARATION FOR USE

4-3. Baud Rate Jumpers

Before installation of the kit it is necessary to determine if the baud rate should be selected by hardwiring in the cable connector, rather than selected by program control. The interface cables HP Part No. 12966-60004, 12966-60006 and 12966-60007 are shipped configured for program control of the baud rate. The 12966-60008 is shipped hardwire configured for use of an external clock. If the hardwired method is preferred, disassemble the cable connector which fastens to the interface printed circuit assembly, and connect the jumpers for the required baud rate. Figure 4-1 and table 4-1 provide instructions to accomplish this.

4-4. INSTALLATION

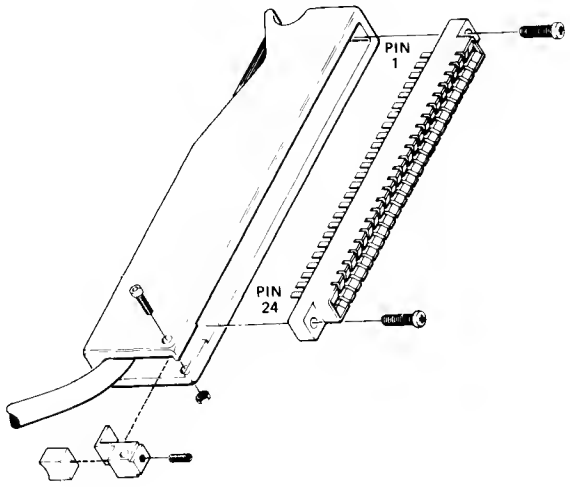
4-5. Printed Circuit Assembly

The printed circuit assembly fits into an I/O slot of the computer's card cage. The I/O slots correspond to I/O select codes which are used during programming to address a particular I/O device. Further information on the computer's I/O system and select codes can be found in your Computer Series Reference Manual.

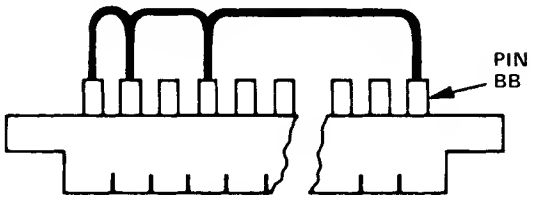
Specific instructions for installing the printed circuit assembly into the computer are contained in your Computer Series Installation and Service Manual.

Table 4-1. Jumper Connections for Baud Transfer Rates

BAUD RATE	BIT PATTERN	CONNECT +5V (PIN 8) TO PINS:	CONNECT SIGNAL GROUND (PINS 1, A, 24, OR BB) TO PINS:
External Clock (X16)	0000	N	12,13,14,15
50	0001	14,N	12,13,15
75	0010	13,N	12,14,15
110	0011	13,14,N	12,15
134.5	0100	12,N	13,14,15
150	0101	12,14,N	13,15
300	0110	12,13,N	14,15
600	0111	12,13,14,N	15
900	1000	15,N	12,13,14
1200	1001	14,15,N	12,13
1800	1010	13,15,N	12,14
2400	1011	13,14,15,N	12
3600	1100	12,15,N	13,14
4800	1101	12,14,15,N	13
7200	1110	12,13,15,N	14
9600	1111	12,13,14,15,N	–



DISASSEMBLY AND ASSEMBLY



48-PIN CONNECTOR

1. DISASSEMBLE CABLE CONNECTOR P1 AS SHOWN IN TOP SECTION OF THIS FIGURE.
2. CONNECT PINS 12, 13, 14, AND 15 TO +5 VOLTS (PIN 8) OR SIGNAL GROUND (PINS 1, A, 24, OR BB, AS CONVENIENT) TO PRODUCE THE SELECTED BAUD RATE AS GIVEN IN TABLE 4-1. USE INSULATED WIRE AND CONNECT ONE PIN TO THE NEXT (OF THE SAME LEVEL: +5V OR GND) UNTIL ALL THE APPROPRIATE PINS ARE CONNECTED TOGETHER. REFER TO BOTTOM SECTION OF THIS FIGURE.

Figure 4-1. Baud Rate Jumper Instructions

4-6. Cable Installation

Connector P1 on the cable assembly connects to the buffered asynchronous data communications PCA. Be sure to position the connector in the proper direction on the PCA as described in manuals referenced above for installing the PCA.

Connector P2 on the cable assembly mates with a connector on the device for which the kit option is intended. The device connectors are located at the rear panel on the HP 2600 and HP 2615. For the HP 264X, the cable connector mates with a printed circuit assembly (PCA) edge connector inside the hinged rear panel of the terminal. The cable connector is polarized so that it can only be inserted onto the PCA connector in one direction.

The exception to the above rules is for cable 12966-60012 (figure 4-8) used with the HP 7221A Plotter Subsystem, P1 is connected to the HP 264X Terminal and P2 to the terminal connector on the plotter.

Wire lists of the four cables are given in tables 4-2 through 4-8. Note that not all of the conductors are used in each cable.

4-7. Performance Test

After installing the kit, proper operation should be verified by performing the diagnostic test. The test connector supplied with the kit replaces the device and device cable during diagnostic testing. Procedures for performing the diagnostic tests are contained in the HP 12966A Buffered Asynchronous Communications Interface Diagnostic Reference Manual, part no. 12966-90004.

4-8. Driver Configuration and Installation

Refer to your operating system manual for driver configuration and installation.

4-9. SERVICING

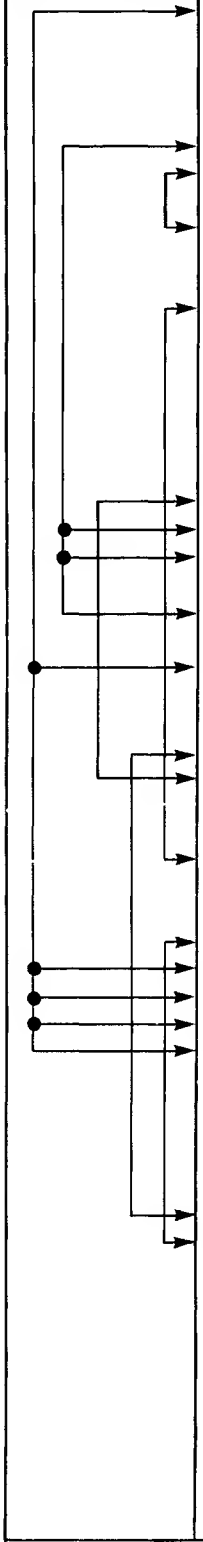
If the kit is not functioning properly, run the diagnostic to verify whether or not the cause is a hardware malfunction. If a hardware problem exists, call the nearest Hewlett-Packard Sales and Service Office and arrange for a board exchange. Continuity checks of the cable can be made using the appropriate wire list (see tables 4-2 through 4-8). Additional checks can be made utilizing schematic and timing diagrams located in Section V.

Table 4-2. Interface Cable (HP2600 and HP 2615 Terminals), part no. 12966-60004, Wire List

HOOD CONNECTOR P1 JUMPERS	(PCA) P1 PIN	SIGNAL NAME (SEE NOTE)	(DEVICE) P2 PIN	WIRE COLOR	RS-232-C CIRCUIT	SIGNAL SOURCE
	A	Signal Ground (EIA)	7	GRN	AB	Common
	B	F				
	C	CA Inhibit				
	D	Transmit Data (EIA)	3	BRN	BA	Intfc
	E	Request to Send (EIA)			CA	
	F	Data Terminal Ready (EIA)			CD	
	H	Ext Freq				
	J	F/4				
	K	F/8				
	L	F/16				
	M	F/2				
	N	P/Ext				
	P	BSBA				
	R	Ext Clock	16	WHT/BLK		Device
	S	Received Data (EIA)	2	BLK	BB	Device
	T	Secondary Line Sig Det (EIA)			SCF	
	U	(spare) (EIA)				
	V	Secondary Receive Data (EIA)			SBB	
	W	BSCA				
	X	Clear to Send (EIA)			CB	
	Y	Data Set Ready (EIA)			CC	
	Z	Ring Indicator (EIA)			CE	
	AA	Receive Line Sig Det (EIA)			CF	
	BB	Signal Ground				
	1	Signal Ground				
	2	CCNT 7				
	3	SXX (Secondary Chan) (EIA)			SBA/SCA	
	4	BSCF				
	5	SIN				
	6	Xmit Data In				
	7	TTY OUT				
	8	+5 volts				
	9	TTY IN				
	10	+12 volts	5,6	ORN,YEL		Intfc
	11	UCLK0				
	12	CLKP2				
	13	CLKP1				
	14	CLKP0				
	15	CLKP3				
	16	Recd Data Out				
	17	BSBB				
	18	DIAG				
	19	Spare				
	20	Run Disable				
	21	BSXX				
	22	UCLK				
	23	-12 volts				
	24	Signal Ground				
	—		4	RED		
	—		8	BLU		
	—		12	VIO		
	—		15	WHT		
	—		17	WHT/BRN		
	—		19	WHT/RED		
	—		20	WHT/ORN		
	—		22	WHT/YEL		

Note: Signals identified by "(EIA)" after the signal name operate at signal levels specified by EIA Standard RS232C (i.e., OFF < -3V, ON > +3V). All other signals operate at TTL logic levels (i.e., approximately, OFF < +1V, ON > +1.5V).

Table 4-3. Interface Cable (HP 264X Terminal), part no. 12966-60008, Wire List



HOOD CONNECTOR P1 JUMPERS	(PCA) P1 PIN	SIGNAL NAME (SEE NOTE)	(DEVICE) P2 PIN	WIRE COLOR	RS-232-C CIRCUIT	SIGNAL SOURCE
	A	Signal Ground (EIA)	H	GRN	AB	Common
	B	F				
	C	CA Inhibit				
	D	Transmit Data (EIA)	C	RED	BA	Intfc
	E	Request to Send (EIA)			CA	
	F	Data Terminal Ready (EIA)			CD	
	H	Ext Freq				
	J	F/4				
	K	F/8				
	L	F/16				
	M	F/2				
	N	P/Ext				
	P	BSBA				
	R	Ext Clock	L	BLU		Device
	S	Received Data (EIA)	B	BRN	BB	Device
	T	Secondary Line Sig Det (EIA)			SCF	
	U	(spare) (EIA)				
	V	Secondary Receive Data (EIA)			SBB	
	W	BSCA				
	X	Clear to Send (EIA)			CB	
	Y	Data Set Ready (EIA)			CC	
	Z	Ring Indicator (EIA)	D	YEL	CE	Device
	AA	Receive Line Sig Det (EIA)			CF	
	BB	Signal Ground				
	1	Signal Ground				
	2	CCNT 7				
	3	SXX (Secondary Chan) (EIA)	E,J	ORN	SBA/SCA	Intfc
	4	BSCF				
	5	SIN				
	6	Xmit Data In				
	7	TTY OUT				
	8	+5 volts				
	9	TTY IN				
	10	+12 volts				
	11	UCLK0				
	12	CLKP2				
	13	CLKP1				
	14	CLKP0				
	15	CLKP3				
	16	Recd Data Out				
	17	BSBB				
	18	DIAG				
	19	Spare				
	20	Run Disable				
	21	BSXX				
	22	UCLK				
	23	-12 volts				
	24	Signal Ground				

Note: Signals identified by "(EIA)" after the signal name operate at signal levels specified by EIA Standard RS232C (i.e., OFF $<-3V$, ON $>+3V$). All other signals operate at TTL logic levels (i.e., approximately, OFF $<+1V$, ON $>+1.5V$).

Table 4-4. Interface Cable (Modem), part no. 12966-60006, Wire List

HOOD CONNECTOR P1 JUMPERS	(PCA) P1 PIN	SIGNAL NAME (SEE NOTE)	(DEVICE) P2 PIN	WIRE COLOR	RS-232-C CIRCUIT	SIGNAL SOURCE
	A	Signal Ground (EIA)	7	GRN	AB	Common
	B	F				
	C	CA Inhibit				
	D	Transmit Data (EIA)	2	BLK	BA	Intfc
	E	Request to Send (EIA)	4	RED	CA	Intfc
	F	Data Terminal Ready (EIA)	20	WHT/ORN	CD	Intfc
	H	Ext Freq				
	J	F/4				
	K	F/8				
	L	F/16				
	M	F/2				
	N	P/Ext				
	P	BSBA				
	R	Ext Clock				
	S	Received Data (EIA)	3	BRN	BB	Device
	T	Secondary Line Sig Det (EIA)	12	VIO	SCF	Device
	U	(spare) (EIA)				
	V	Secondary Receive Data (EIA)			SBB	
	W	BSCA				
	X	Clear to Send (EIA)	5	ORN	CB	Device
	Y	Data Set Ready (EIA)	6	YEL	CC	Device
	Z	Ring Indicator (EIA)	22	WHT/YEL	CE	Device
	AA	Receive Line Sig Det (EIA)	8	BLU	CF	Device
	BB	Signal Ground				
	1	Signal Ground				
	2	CCNT 7				
	3	SXX (Secondary Chan) (EIA)	–	GRA	SBA/SCA	
	4	BSCF				
	5	SIN				
	6	Xmit Data In				
	7	TTY OUT				
	8	+5 volts				
	9	TTY IN				
	10	+12 volts				
	11	UCLK0				
	12	CLKP2				
	13	CLKP1				
	14	CLKP0				
	15	CLKP3				
	16	Recd Data Out				
	17	BSBB				
	18	DIAG				
	19	Spare				
	20	Run Disable				
	21	BSXX				
	22	UCLK				
	23	–12 volts				
	24	Signal Ground				
	–		15	WHT		
	–		16	WHT/BLK		
	–		17	WHT/BRN		
	–		19	WHT/RED		

Note: Signals identified by "(EIA)" after the signal name operate at signal levels specified by EIA Standard RS232C (i.e., OFF < –3V, ON > +3V). All other signals operate at TTL logic levels (i.e., approximately, OFF < +1V, ON > 1.5V).

Table 4-5. Interface Cable (HP 2749B Teleprinter), part no. 12966-60007, Wire List

HOOD CONNECTOR P1 JUMPERS	(PCA) P1 PIN	SIGNAL NAME (SEE NOTE)	(DEVICE) P2 PIN	WIRE COLOR	RS-232-C CIRCUIT	SIGNAL SOURCE
	A	Signal Ground (EIA)	1,7	BLK	AB	Common
	B	F				
	C	CA Inhibit				
	D	Transmit Data (EIA)	3	YEL	BA	Intfc
	E	Request to Send (EIA)			CA	
	F	Data Terminal Ready (EIA)			CD	
	H	Ext Freq				
	J	F/4				
	K	F/8				
	L	F/16				
	M	F/2				
	N	P/Ext				
	P	BSBA				
	R	Ext Clock				
	S	Received Data (EIA)	2	RED	BB	Device
	T	Secondary Line Sig Det (EIA)			SCF	
	U	(spare) (EIA)				
	V	Secondary Receive Data (EIA)			SBB	
	W	BSCA				
	X	Clear to Send (EIA)			CB	
	Y	Data Set Ready (EIA)			CC	
	Z	Ring Indicator (EIA)			CE	
	AA	Receive Line Sig Det (EIA)			CF	
	BB	Signal Ground				
	1	Signal Ground				
	2	CCNT 7				
	3	SXX (Secondary Chan) (EIA)			SBA/SCA	
	4	BSCF				
	5	SIN				
	6	Xmit Data In				
	7	TTY OUT				
	8	+5 volts				
	9	TTY IN				
	10	+12 volts				
	11	UCLK0				
	12	CLKP2				
	13	CLKP1				
	14	CLKP0				
	15	CLKP3				
	16	Recd Data Out				
	17	BSBB				
	18	DIAG				
	19	Spare				
	20	Run Disable				
	21	BSXX				
	22	UCLK				
	23	-12 volts				
	24	Signal Ground				

Note: Signals identified by "(EIA)" after the signal name operate at signal levels specified by EIA Standard RS232C (i.e., OFF < -3V, ON > +3V). All other signals operate at TTL logic levels (i.e., approximately, OFF < +1V, ON > +1.5V).

Table 4-6. Interface Cable (HP 2621 Terminal), part no. 12966-60010, Wire List

HOOD CONNECTOR P1 JUMPERS	(PCA) P1 PIN	SIGNAL NAME (SEE NOTE)	(DEVICE) P2 PIN	WIRE COLOR	RS-232-C CIRCUIT	SIGNAL SOURCE
	A	Signal Ground (EIA)	48	GRN	AB	Common
	B	F				
	C	CA Inhibit				
	D	Transmit Data (EIA)	42	RED	BA	Intfc
	E	Request to Send (EIA)			CA	
	F	Data Terminal Ready (EIA)			CD	
	H	Ext Freq				
	J	F/4				
	K	F/8				
	L	F/16				
	M	F/2				
	N	P/Ext				
	P	BSBA				
	R	Ext Clock	50	BLU		
	S	Received Data (EIA)	12	BRN	BB	Device
	T	Secondary Line Sig Det (EIA)			SCF	Device
	U	(spare) (EIA)				
	V	Secondary Receive Data (EIA)			SBB	
	W	BSCA				
	X	Clear to Send (EIA)			CB	
	Y	Data Set Ready (EIA)			CC	
	Z	Ring Indicator (EIA)	13	YEL	CE	Device
	AA	Receive Line Sig Det (EIA)			CF	
	BB	Signal Ground				
	1	Signal Ground				
	2	CCNT 7				
	3	SXX (Secondary Chan) (EIA)	44	ORG	SBA/SCA	Intfc
	4	BSCF				
	5	SIN				
	6	Xmit Data In				
	7	TTY OUT				
	8	+5 volts				
	9	TTY IN				
	10	+12 volts				
	11	UCLK0				
	12	CLKP2				
	13	CLKP1				
	14	CLKP0				
	15	CLKP3				
	16	Recd Data Out				
	17	BSBB				
	18	DIAG				
	19	Spare				
	20	Run Disable				
	21	BSXX				
	22	UCLK				
	23	-12 volts				
	24	Signal Ground				
			36, 46			

Note: Signals identified by "(EIA)" after the signal name operate at signal levels specified by EIA Standard RS232C (i.e., OFF < -3V, ON > +3V). All other signals operate at TTL logic levels (i.e., approximately, OFF < +1V, ON > +1.5V).

Table 4-7. Interface Cable (HP 7221A Plotter), part no. 12966-60011, Wire List

HOOD CONNECTOR P1 JUMPERS	(PCA) P1 PIN	SIGNAL NAME (SEE NOTE)	(DEVICE) P2 PIN	WIRE COLOR	RS-232-C CIRCUIT	SIGNAL SOURCE
	A	Signal Ground (EIA)	7	GRN	AB	Common
	B	F				
	C	CA Inhibit				
	D	Transmit Data (EIA)	3	ORG	BA	Intfc
	E	Request to Send (EIA)			CA	
	F	Data Terminal Ready (EIA)			CD	
	H	Ext Freq				
	J	F/4				
	K	F/8				
	L	F/16				
	M	F/2				
	N	P/Ext				
	P	BSBA				
	R	Ext Clock	24	YEL		Device
	S	Received Data (EIA)	2	RED	BB	Device
	T	Secondary Line Sig Det (EIA)			SCF	
	U	(spare) (EIA)				
	V	Secondary Receive Data (EIA)			SBB	
	W	BSCA				
	X	Clear to Send (EIA)			CB	
	Y	Data Set Ready (EIA)			CC	
	Z	Ring Indicator (EIA)	19	BLU	CE	Device
	AA	Receive Line Sig Det (EIA)			CF	
	BB	Signal Ground				
	1	Signal Ground				
	2	CCNT 7				
	3	SXX (Secondary Chan) (EIA)	13	BRN	SBA/SCA	Intfc
	4	BSCF				
	5	SIN				
	6	Xmit Data In				
	7	TTY OUT				
	8	+5 volts				
	9	TTY IN				
	10	+12 volts				
	11	UCLK0				
	12	CLKP2				
	13	CLKP1				
	14	CLKP0				
	15	CLKP3				
	16	Recd Data Out				
	17	BSBB				
	18	DIAG				
	19	Spare				
	20	Run Disable				
	21	BSXX				
	22	UCLK				
	23	−12 volts				
	24	Signal Ground				
	—		4, 5			
	—		6, 20			

Note: Signals identified by "(EIA)" after the signal name operate at signal levels specified by EIA Standard RS232C (i.e., OFF < −3V, ON > +3V). All other signals operate at TTL logic levels (i.e., approximately, OFF < +1V, ON > +1.5V).

Table 4-8. Interface Cable (HP 264X Terminal to HP 7221A Plotter), part no. 12966-60012, Wire List

TERMINAL CONNECTOR P1 JUMPERS	TERM P1 PIN	SIGNAL NAME	PLOTTER P2 PIN	WIRE COLOR	RS-232-C CIRCUIT	SIGNAL SOURCE
	B	Transmitted Data	2	RED	BA	Terminal
	C	Received Data	3	ORG	BB	Plotter
	D	Secondary Request to Send	19	BLU	SCA	Terminal
→	E	Secondary Clear to Send	13	BRN	SCB	Plotter
	H	Common Signal ground	7	GRN	AB	Common
→	J					
	L	Ext. Clock	24	YEL		Terminal

DIAGRAMS

SECTION V

5-1. INTRODUCTION

This section provides the component location, block, schematic and timing diagrams to aid in verifying the operational status of the hardware. This assembly is not field repairable, if a hardware problem exists, call the nearest Hewlett-Packard Sales and Service Office to arrange for a board exchange.

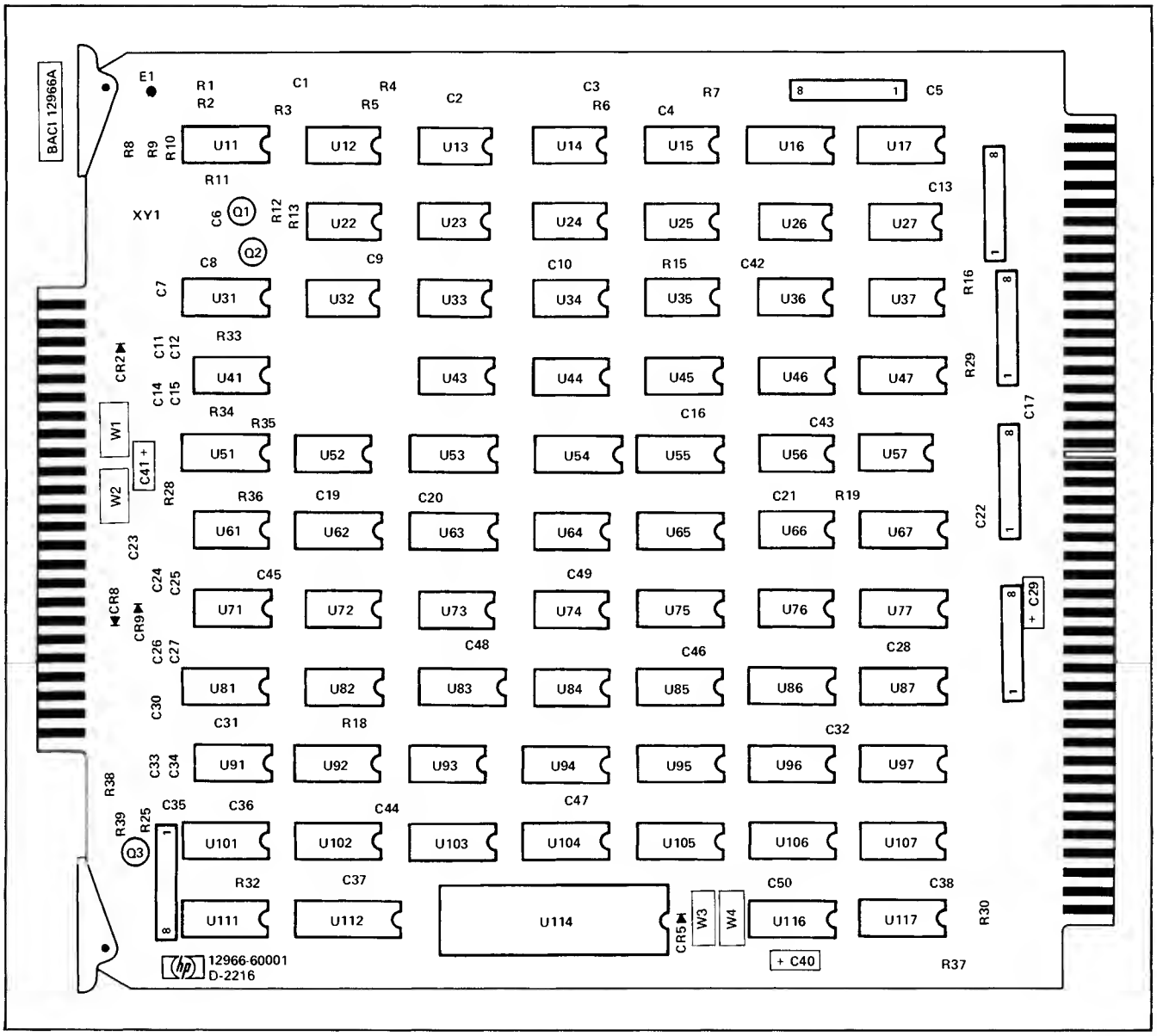


Figure 5-1. HP 12966A Buffered Asynchronous Data Communications Interface Assembly Diagram

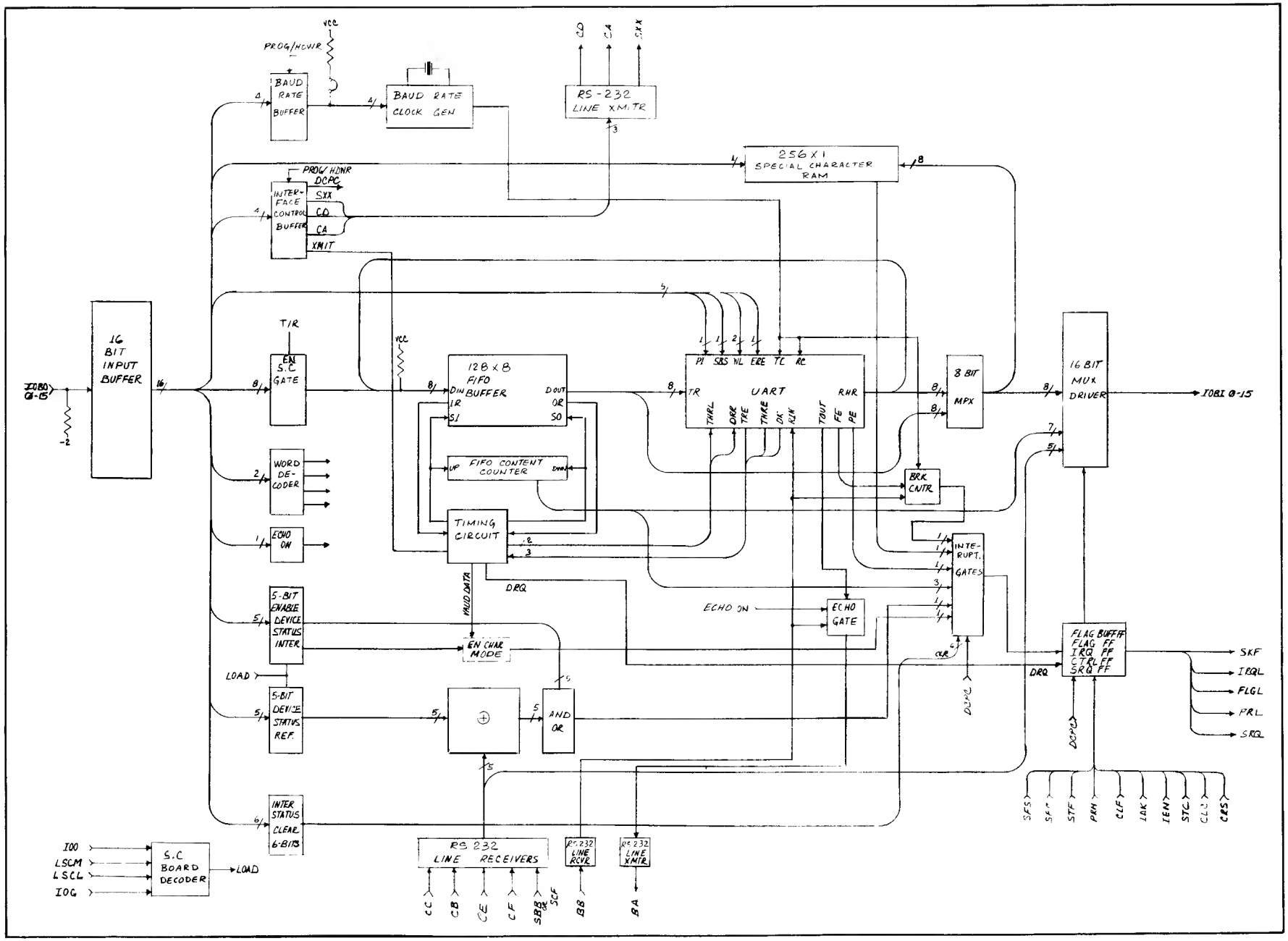


Figure 5-2. HP 12966A Buffered Asynchronous Data Communications Interface Block Diagram

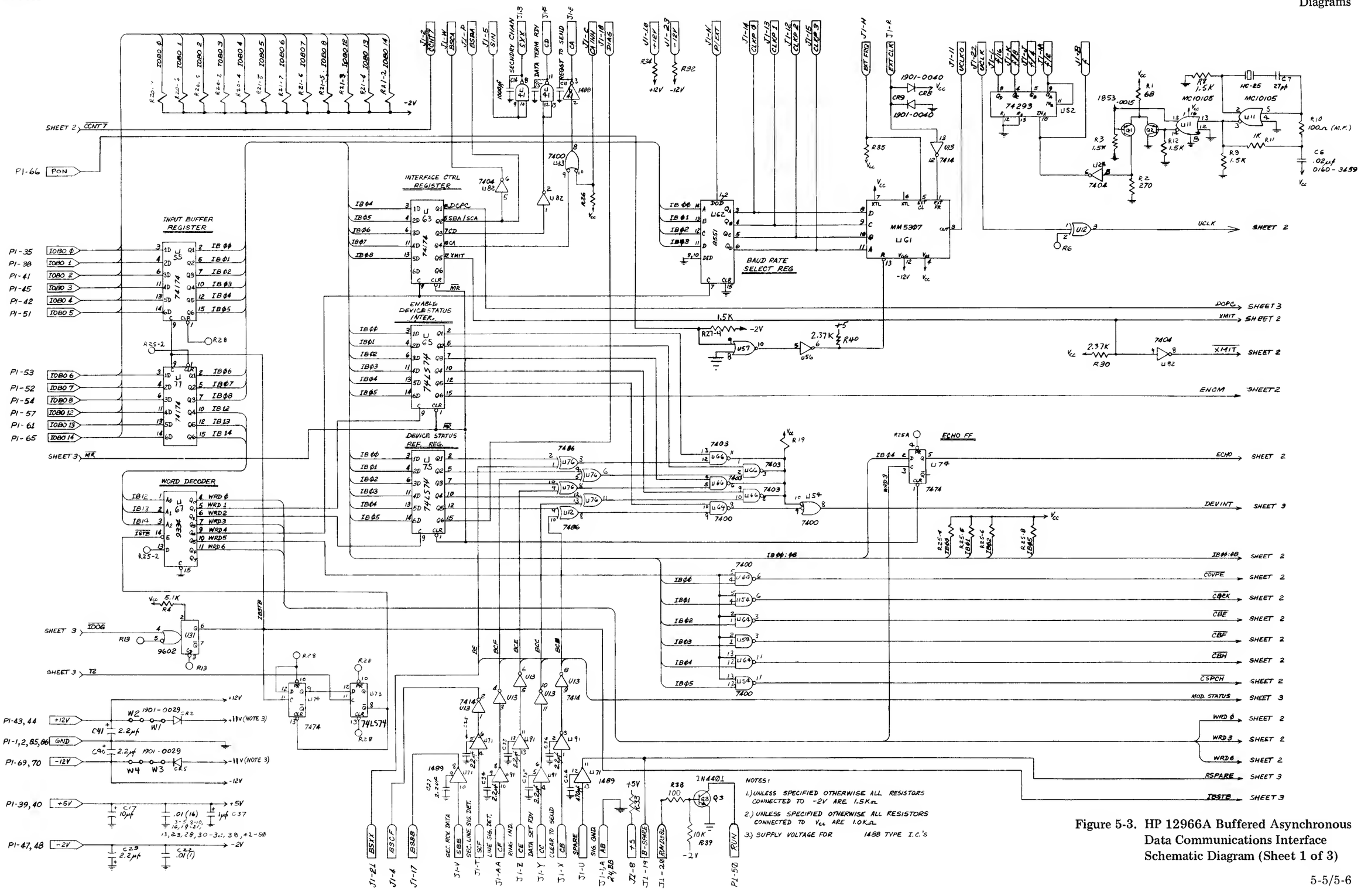


Figure 5-3. HP 12966A Buffered Asynchronous Data Communications Interface Schematic Diagram (Sheet 1 of 3)

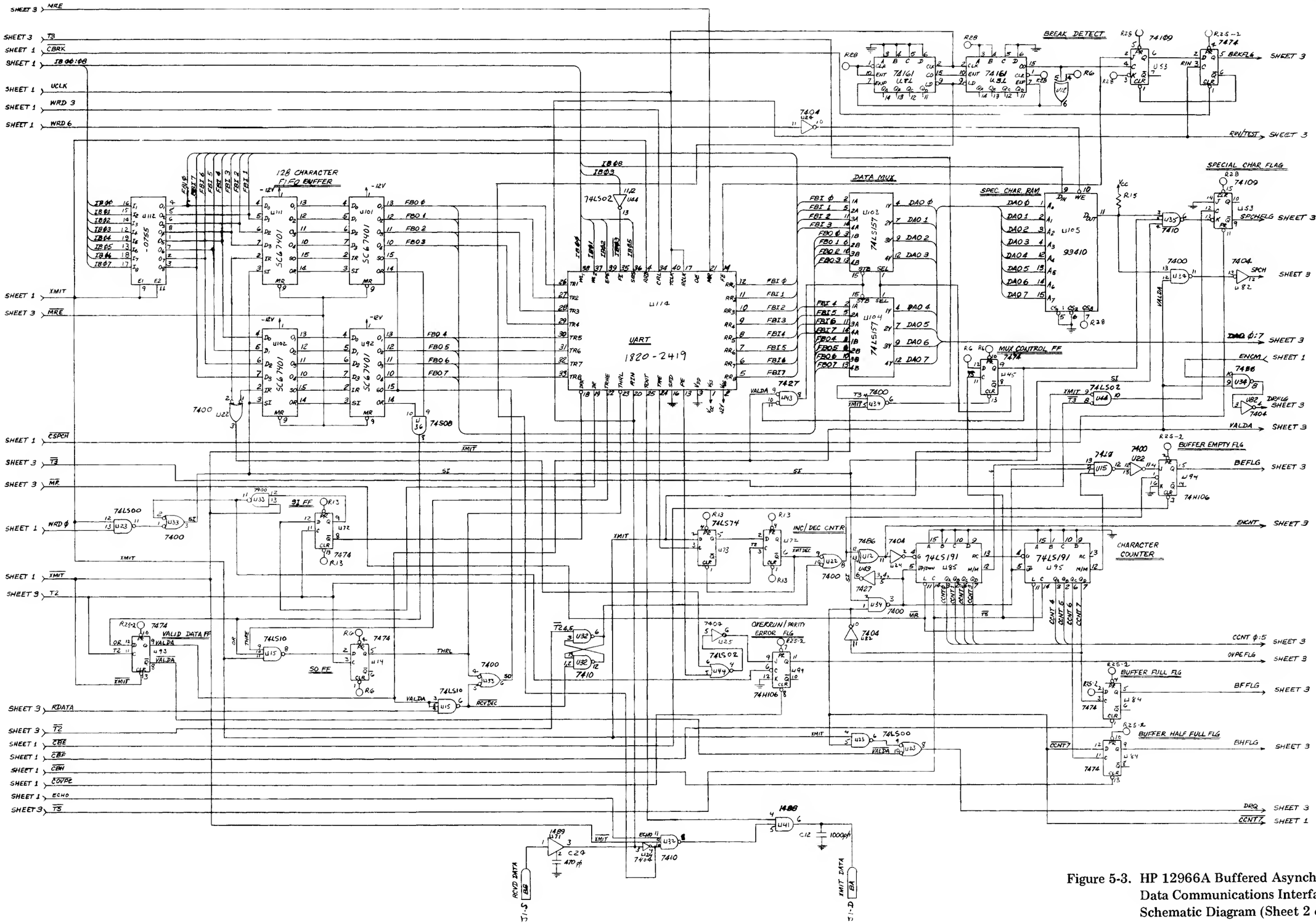


Figure 5-3. HP 12966A Buffered Asynchronous Data Communications Interface Schematic Diagram (Sheet 2 of 3)

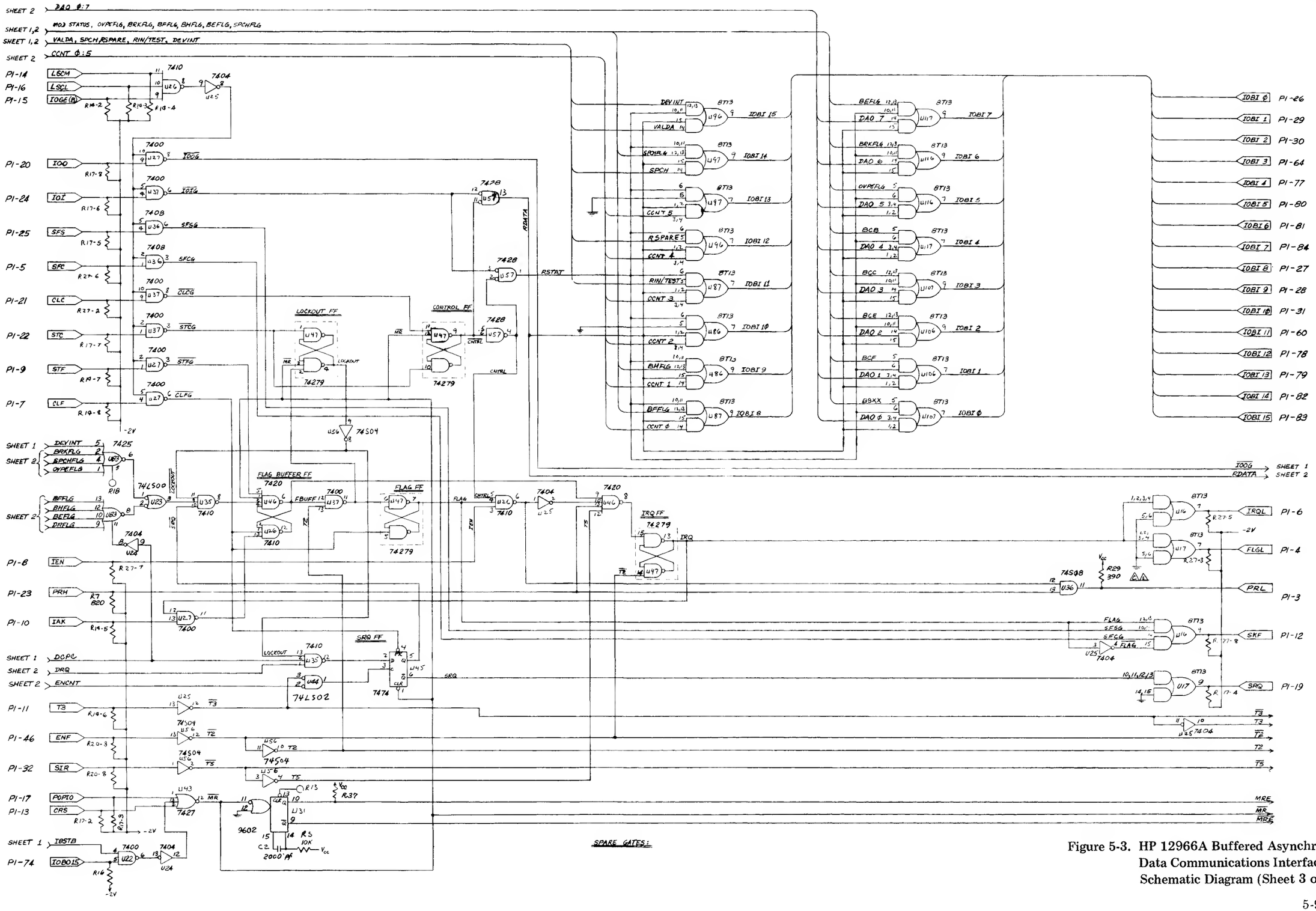


Figure 5-3. HP 12966A Buffered Asynchronous Data Communications Interface Schematic Diagram (Sheet 3 of 3)

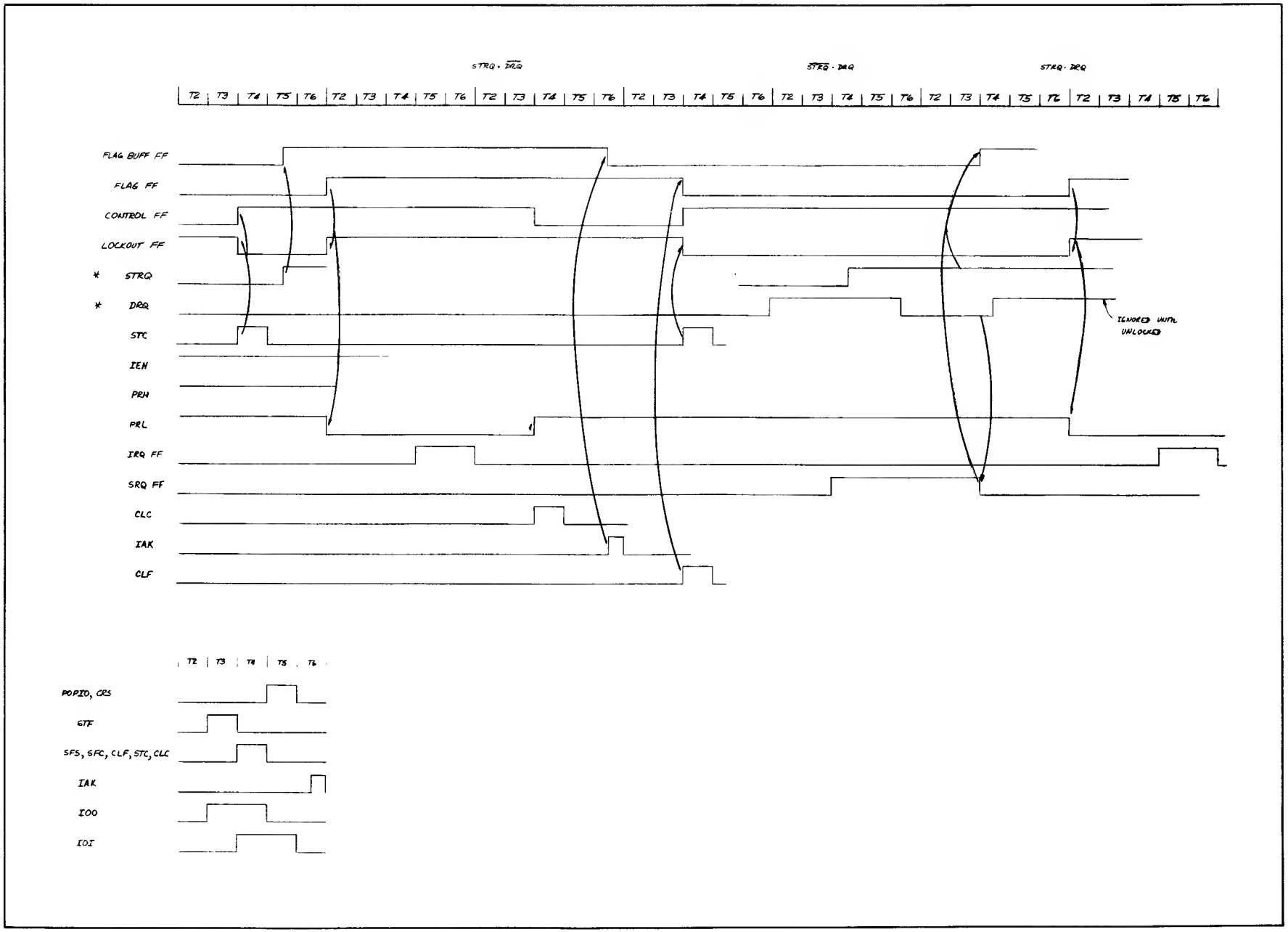


Figure 5-4. HP 12966A Buffered Asynchronous Data Communications Interface Timing Diagram (Sheet 1 of 3)

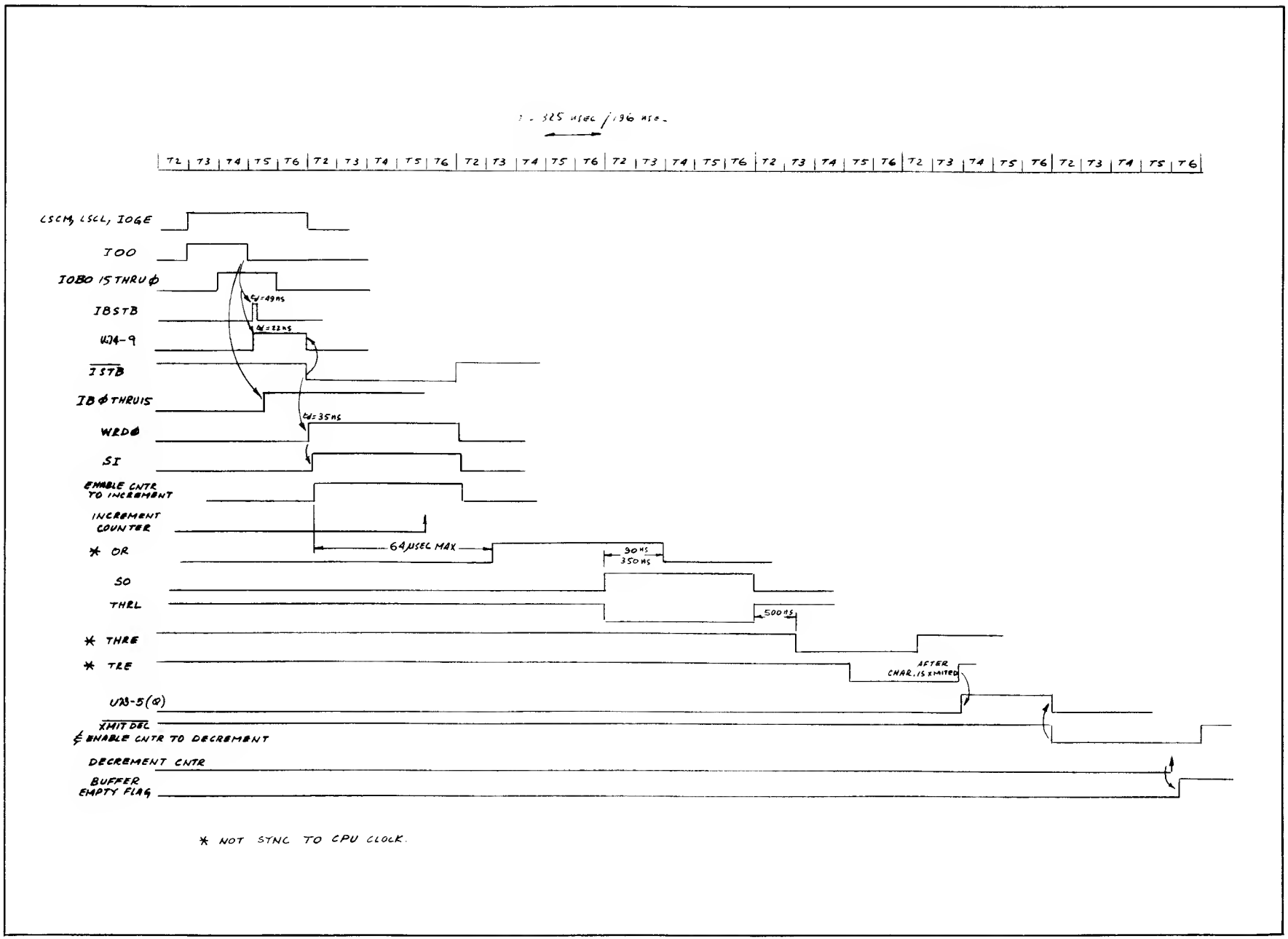


Figure 5-4. HP 12966A Buffered Asynchronous Data Communications Interface Timing Diagram (Sheet 2 of 3)

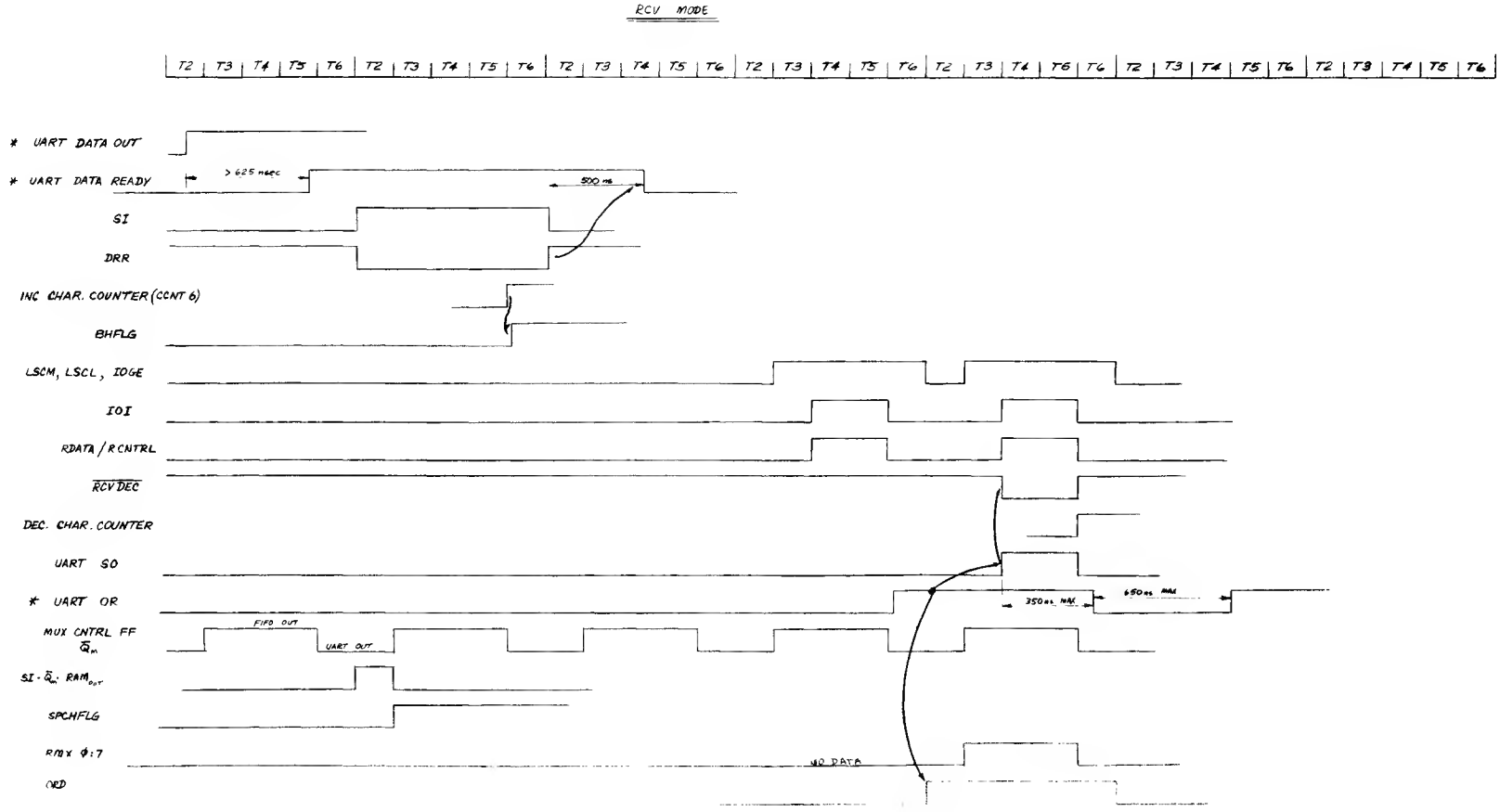


Figure 5-4. HP 12966A Buffered Asynchronous Data Communications Interface Timing Diagram (Sheet 3 of 3)

REPLACEABLE PARTS

SECTION VI

6-1. INTRODUCTION

This chapter contains information for ordering replaceable parts for the HP 12966A assembly. Table 6-1 gives a list of replaceable parts, while table 6-2 cross references the names and address of manufacturers indexed by code number in table 6-1.

6-2. REPLACEABLE PARTS

Table 6-1 contains a list of replaceable parts in reference designation order. The following information is listed for each part:

1. Reference designation of the part.
2. The Hewlett-Packard part number.
3. Part number check digit (CD).
4. Total quantity.
5. Description of the part.
6. A five-digit manufacturer's code number of a typical manufacturer of the part. Refer to table 6-2 for a cross reference of manufacturers.
7. The manufacturer's part number.

6-3. ORDERING INFORMATION

To order replacement parts or to obtain information on parts, address the order or inquiry to the local Hewlett-Packard Sales and Service Office (Sales and Service Offices are listed at the back of this manual).

To order a part, quote the Hewlett-Packard part number (with the check digit), and indicate the quantity required. The check digit will insure accurate and timely processing of your order.

Replaceable Parts

Table 6-1. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
DE A1	12966-60001	5	1	BUFFER ASYNCHRONOUS IF BOARD ASSEMBLY	28480	12966-60001
C2	0160-3457	7	1	CAPACITOR-FXD 2000PF +-10% 250VDC CER	28480	0160-3457
C3	0160-2055	9	27	CAPACITOR-FXD .010F +80-20% 100VDC CER	28480	0160-2055
C4	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C5	0160-2055	9		CAPACITOR-FXD .010F +80-20% 100VDC CER	28480	0160-2055
C6	0160-3459	9	1	CAPACITOR-FXD .02UF +-20% 100VDC CER	28480	0160-3459
C7	0160-2306	3	1	CAPACITOR-FXD 27PF +-5% 300VDC MICA	28480	0160-2306
C8	0160-2055	9		CAPACITOR-FXD .010F +80-20% 100VDC CER	28480	0160-2055
C9	0160-2055	9		CAPACITOR-FXD .010F +80-20% 100VDC CER	28480	0160-2055
C10	0160-2055	9		CAPACITOR-FXD .010F +80-20% 100VDC CER	28480	0160-2055
C11	0160-3456	6	4	CAPACITOR-FXD 1000PF +-10% 1KVDC CER	28480	0160-3456
C12	0160-3456	6		CAPACITOR-FXD 1000PF +-10% 1KVDC CER	28480	0160-3456
C13	0160-2055	9		CAPACITOR-FXD .010F +80-20% 100VDC CER	28480	0160-2055
C14	0160-3456	6		CAPACITOR-FXD 1000PF +-10% 1KVDC CER	28480	0160-3456
C15	0160-3456	6		CAPACITOR-FXD 1000PF +-10% 1KVDC CER	28480	0160-3456
C16	0160-2055	9		CAPACITOR-FXD .010F +80-20% 100VDC CER	28480	0160-2055
C17	0180-0374	3	1	CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C19	0160-2055	9		CAPACITOR-FXD .010F +80-20% 100VDC CER	28480	0160-2055
C20	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C21	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C22	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C23	0160-2055	9		CAPACITOR-FXD .010F +80-20% 100VDC CER	28480	0160-2055
C24	0160-3455	5	2	CAPACITOR-FXD 470PF +-10% 1KVDC CER	28480	0160-3455
C25	0160-5107	8	6	CAPACITOR-FXD 2.2UF +-20% 50VDC CER	28480	0160-5107
C26	0160-3455	5		CAPACITOR-FXD 470PF +-10% 1KVDC CER	28480	0160-3455
C27	0160-5107	8		CAPACITOR-FXD 2.2UF +-20% 50VDC CER	28480	0160-5107
C28	0160-2055	9		CAPACITOR-FXD .010F +80-20% 100VDC CER	28480	0160-2055
C29	0180-0197	8	3	CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
C30	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C31	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C32	0160-2055	9		CAPACITOR-FXD .010F +80-20% 100VDC CER	28480	0160-2055
C33	0160-5107	8		CAPACITOR-FXD 2.2UF +-20% 50VDC CER	28480	0160-5107
C34	0160-5107	8		CAPACITOR-FXD 2.2UF +-20% 50VDC CER	28480	0160-5107
C35	0160-5107	8		CAPACITOR-FXD 2.2UF +-20% 50VDC CER	28480	0160-5107
C36	0160-5107	8		CAPACITOR-FXD 2.2UF +-20% 50VDC CER	28480	0160-5107
C37	0160-0127	2	1	CAPACITOR-FXD 1UF +-20% 25VDC CER	28480	0160-0127
C38	0160-2055	9		CAPACITOR-FXD .010F +80-20% 100VDC CER	28480	0160-2055
C40	0180-0197	8		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
C41	0180-0197	8		CAPACITOR-FXD 2.2UF+-10% 20VDC TA	56289	150D225X9020A2
C42	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C43	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C44	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C45	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C46	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C47	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C48	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
C49	0160-2055	9		CAPACITOR-FXD .010F +80-20% 100VDC CER	28480	0160-2055
C50	0160-2055	9		CAPACITOR-FXD .010F +80-20% 100VDC CER	28480	0160-2055
CR2	1901-0029	6	2	DIODE-PWR RECT 600V 750MA DO-29	28480	1901-0029
CR5	1901-0029	6		DIODE-PWR RECT 600V 750MA DO-29	28480	1901-0029
CR8	1901-0040	1	2	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR9	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
Q1	1853-0015	7	2	TRANSISTOR PNP SI PD=200MW FT=500MHZ	28480	1853-0015
Q2	1853-0015	7		TRANSISTOR PNP SI PD=200MW FT=500MHZ	28480	1853-0015
Q3	1854-0467	5	1	TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	03508	2N4401
R1	0757-0397	3	1	RESISTOR 68.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-68R1-F
R2	0683-2715	6	1	RESISTOR 270 5% .25W FC TC=-400/+600	01121	CB2715
R3	0757-1094	9	5	RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
R4	0757-0438	3	1	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
R5	0757-0442	9	2	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R6	0757-0280	3	11	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R7	0683-8215	3	1	RESISTOR 820 5% .25W FC TC=-400/+600	01121	CB8215
R8	0757-1094	9		RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
R9	0757-1094	9		RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
R10	0757-0401	0	2	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
R11	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R12	0757-1094	9		RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
R13	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R14	1810-0020	4	5	NETWORK-RES 8-SIP1.5K OHM X 7	28480	1810-0020
R15	0757-0200	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R16	0757-1094	9		RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
R17	1810-0020	4		NETWORK-RES 8-SIP1.5K OHM X 7	28480	1810-0020
R18	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R19	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R20	1810-0020	4		NETWORK-RES 8-SIP1.5K OHM X 7	28480	1810-0020

See introduction to this section for ordering information
*Indicates factory selected value

Replaceable Parts

Table 6-1. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
R21	1810-0020	4		NETWORK-RES 8-SIP1.5K OHM X 7	28480	1810-0020
R25	1810-0030	6	1	NETWORK-RES 8-SIP1.0K OHM X 7	28480	1810-0030
R27	1810-0020	4		NETWORK-RES 8-SIP1.5K OHM X 7	28480	1810-0020
R28	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R29	0683-3915	0	1	RESISTOR 390 5% .25W FC TC=-400/+600	01121	CB3915
R30	0698-3150	6	3	RESISTOR 2.37K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2371-F
R32	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R33	0757-0416	7	1	RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
R34	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R35	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R36	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R37	0698-3150	6		RESISTOR 2.37K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2371-F
R38	0757-0401	8		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-100-F
R39	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R40	0698-3150	6		RESISTOR 2.37K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2371-F
U11	1820-0803	2	1	IC GATE ECL OR-NOR TPL	04713	MC10105P
U12	1820-0282	1	2	IC GATE TTL EXCL-OR QUAD 2-INP	01295	SN7486N
U13	1820-1053	6	1	IC SCHMITT-TRIG TTL INV HEX	01295	SN7414N
U14	1820-0077	2	6	IC FF TTL D-TYPE POS-EDGE-TRIG CLEAR	01295	SN7474N
U15	1820-1202	7	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
U16	1820-1080	9	10	IC DRVR TTL LINE DRVR DUAL 6-INP	01295	SN75121N SELECTED
U17	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	01295	SN75121N SELECTED
U22	1820-0054	5	7	IC GATE TTL NAND QUAD 2-INP	01295	SN7400N
U23	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U24	1820-0174	0	3	IC INV TTL HEX	01295	SN7404N
U25	1820-0174	0		IC INV TTL HEX	01295	SN7404N
U26	1820-0068	1	3	IC GATE TTL NAND TPL 3-INP	01295	SN7410N
U27	1820-0054	5		IC GATE TTL NAND QUAD 2-INP	01295	SN7400N
U31	1820-0515	3	1	IC MV TTL MONOSTBL RETRIG/RESET DUAL	04713	MC8602P
U32	1820-0068	1		IC GATE TTL NAND TPL 3-INP	01295	SN7410N
U33	1820-0054	5		IC GATE TTL NAND QUAD 2-INP	01295	SN7400N
U34	1820-0054	5		IC GATE TTL NAND QUAD 2-INP	01295	SN7400N
U35	1820-0068	1		IC GATE TTL NAND TPL 3-INP	01295	SN7410N
U36	1820-1367	5	1	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U37	1820-0054	5		IC GATE TTL NAND QUAD 2-INP	01295	SN7400N
U41	1820-0509	5	1	IC DRVR DTL LINE DRVR QUAD	04713	MC1488L
U43	1820-0782	6	1	IC GATE TTL NOR TPL 3-INP	01295	SN7427N
U44	1820-0328	6	1	IC GATE TTL NOR QUAD 2-INP	01295	SN7402N
U45	1820-0077	2		IC FF TTL D-TYPE POS-EDGE-TRIG CLEAR	01295	SN7474N
U46	1820-0069	2	1	IC GATE TTL NAND DUAL 4-INP	01295	SN7420N
U47	1820-1089	8	1	IC LCH TTL QUAD	01295	SN74279N
U51	1820-0716	6	2	IC CNTR TTL BIN SYNCHRO POS-EDGE-TRIG	01295	SN74161N
U52	1820-1264	1	1	IC CNTR TTL BIN ASYNCHRO NEG-EDGE-TRIG	01295	SN74293N
U53	1820-1116	2	1	IC FF TTL J-K BAR POS-EDGE-TRIG	01295	SN74109N
U54	1820-0054	5		IC GATE TTL NAND QUAD 2-INP	01295	SN7400N
U55	1820-0788	2	3	IC FF TTL D-TYPE POS-EDGE-TRIG CLEAR HEX	01295	SN74174N
U56	1820-0683	6	1	IC INV TTL S HEX 1-INP	01295	SN74S04N
U57	1820-1184	4	1	IC BFR TTL NOR QUAD 2-INP	01295	SN7428N
U61	1820-1348	2	1	IC GEN PMOS	27014	MM5307N
U62	1820-0574	4	1	IC RGTR TTL D-TYPE 4-BIT	01295	SN74173N
U63	1820-0788	2		IC FF TTL D-TYPE POS-EDGE-TRIG CLEAR HEX	01295	SN74174N
U64	1820-0054	5		IC GATE TTL NAND QUAD 2-INP	01295	SN7400N
U65	1820-1196	0	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
U66	1820-0269	4	1	IC GATE TTL NAND QUAD 2-INP	01295	SN7403N
U67	1820-0833	8	1	IC LCH TTL COM CLEAR 8-BIT	07263	9334PC
U71	1820-0990	8	2	IC RCVR DTL NAND LINE QUAD	01295	SN75189AJ
U72	1820-0077	2		IC FF TTL D-TYPE POS-EDGE-TRIG CLEAR	01295	SN7474N
U73	1820-1112	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U74	1820-0077	2		IC FF TTL D-TYPE POS-EDGE-TRIG CLEAR	01295	SN7474N
U75	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
U76	1820-0282	1		IC GATE TTL EXCL-OR QUAD 2-INP	01295	SN7486N
U77	1820-0788	2		IC FF TTL D-TYPE POS-EDGE-TRIG CLEAR HEX	01295	SN74174N
U81	1820-0716	6		IC CNTR TTL BIN SYNCHRO POS-EDGE-TRIG	01295	SN74161N
U82	1820-0174	0		IC INV TTL HEX	01295	SN7404N
U83	1820-0655	2	1	IC GATE TTL NOR DUAL 4-INP	01295	SN7425N
U84	1820-0077	2		IC FF TTL D-TYPE POS-EDGE-TRIG CLEAR	01295	SN7474N
U85	1820-0545	9	2	IC CNTR TTL BIN UP/DOWN SYNCHRO	01295	SN74191N
U86	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	01295	SN75121N SELECTED
U87	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	01295	SN75121N SELECTED
U91	1820-0990	8		IC RCVR DTL NAND LINE QUAD	01295	SN75189AJ
U92	1816-1536	1	4	IC-FIFO SC67401	28480	1816-1536
U93	1820-0077	2		IC FF TTL D-TYPE POS-EDGE-TRIG CLEAR	01295	SN7474N
U94	1820-0715	5	1	IC FF TTL H J-K NEG-EDGE-TRIG	01295	SN74H106N
U95	1820-0545	9		IC CNTR TTL BIN UP/DOWN SYNCHRO	01295	SN74191N
U96	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	01295	SN75121N SELECTED

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-1. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U97	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	01295	SN75121N SELECTED
U101	1816-1536	1		IC-FIFO SC67401	28480	1816-1536
U102	1816-1536	1		IC-FIFO SC67401	28480	1816-1536
U103	1820-1470	1	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
U104	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
U105	1820-0988	4	1	IC TTL 256-BIT STAT RAM 60-NS 0-C	07263	93410DC
U106	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	01295	SN75121N SELECTED
U107	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	01295	SN75121N SELECTED
U111	1816-1536	1		IC-FIFO SC67401	28480	1816-1536
U112	1820-0755	3	1	IC DRVR TTL OCTL	28480	1820-0755
U114	1820-2419	0	1	IC UART PMOS	52840	TR1863A
U116	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	01295	SN75121N SELECTED
U117	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	01295	SN75121N SELECTED
W1	8159-0005	0	4	RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
W2	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
W3	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
W4	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
XY1	1200-0546	6	1	SOCKET-XTAL 2-CONT HC-25/U DIP-SLDR	28480	1200-0546
Y1	0410-0587	9	1	CRYSTAL- 7.373 MHZ	28480	0410-0507
				MISCELLANEOUS PARTS		
	0360-0294	8	2	TERMINAL-STUD SGL-TOR SWGFRM-MTG	28480	0360-0294
	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
	1810-0072	6	1	NETWORK-RES 8-SIP2.37K OHM X 7	28480	1810-0072
	1820-1144	6	1	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
	1820-1278	7	2	IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS191N
	5040-6001	4	1	EXTRACTOR-P.C BOARD	28480	5040-6001
	5040-6065	0	1	EXTRACTOR-P.C. BOARD (RED)	28480	5040-6065

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Manufacturer's Code List

MFR NO.	MANUFACTUER NAME	ADDRESS		ZIP CODE
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
03508	GE CO SEMICONDUCTOR PROD DEPT	AUBURN	NY	13201
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85008
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA	CA	95051
28480	HEWLETT-PACKARD CO CORP HQ	PALO ALTO	CA	94304
52840	WESTERN DIGITAL CORP	NEWPORT BEACH	CA	92626
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247

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SALES & SUPPORT OFFICES

Arranged Alphabetically by Country

Product Line Sales/Support Key

Key	Product Line
A	Analytical
CM	Components
C	Computer Systems Sales only
CH	Computer Systems Hardware Sales and Services
CS	Computer Systems Software Sales and Services
E	Electronic Instruments & Measurement Systems
M	Medical Products
MP	Medical Products Primary SRO
MS	Medical Products Secondary SRO
P	Personal Computation Products
*	Sales only for specific product line
**	Support only for specific product line

IMPORTANT: These symbols designate general product line capability. They do not insure sales or support availability for all products within a line, at all locations. Contact your local sales office for information regarding locations where HP support is available for specific products.

HP distributors are printed in italics.

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6

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